

Printed Low-Voltage Organic Transistors on Plastics and Paper

Daniel Tobjörk



Physics
Department of Natural Sciences
Center for Functional Materials
Graduate School of Materials Research
Åbo Akademi University
Åbo, Finland



Supervisor

Professor Ronald Österbacka
Åbo Akademi University

Pre-examiners

Professor Magnus Berggren
Linköping University

Professor Donald Lupo
Tampere University of Technology

Opponent for the public defense

Professor Ananth Dodabalapur
The University of Texas at Austin

Den rätta vägen är inte en sträcka,
det är att sjunga medan man går.

Erik Rådbo

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List of included publications

- Paper I.** *Low-Voltage Organic Transistors Fabricated Using Reverse Gravure Coating on Prepatterned Substrates*
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- Paper III.** *Absence of substrate roughness effects on an all-printed organic transistor operating at one volt*
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- Paper IV.** *IR-sintering of ink-jet printed metal-nanoparticles on paper*
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- Paper V.** *A multilayer coated fiber-based substrate suitable for printed functionality*
R. Bollström, A. Määttänen, D. Tobjörk, P. Ihalainen,
N. Kaihovirta, R. Österbacka, J. Peltonen and M. Toivakka
Organic Electronics **10**, 1020–1023 (2009).
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Author's contribution

The author of this thesis had an active role in all stages of the work presented in this thesis, including the initial development processes of planning and executing experiments, analyzing data, discussing results and drawing conclusions. Some of the particular contributions to the papers included in this thesis are listed below.

- Paper I.** The author of this thesis used the reverse gravure coating technique for fabricating transistors and studied the film thicknesses by optical methods. The manuscript was written by N. J. Kaihovirta and the author of this thesis, and was finalized together with the other co-authors of the paper.
- Paper II.** The author developed a printing process for the transistors and investigated the printed structures by x-ray photoelectron spectroscopy. The manuscript was written by the author and was finalized together with the co-authors.
- Paper III.** The author of this thesis printed the transistors and investigated the effects of the substrate together with N. J. Kaihovirta, who also wrote the manuscript and finalized it together with the co-authors.
- Paper IV.** All of the theoretical and experimental work was made by the author, except that concerning the gold-nanoparticle synthesis and paper fabrication, which was made by P. Pulkkinen and R. Bollström, respectively. The manuscript was written by the author and was finalized together with the co-authors.
- Paper V.** The author of this thesis was active in the development process of the paper substrate and did all the experimental work with the transistors. The first draft of the manuscript was written by R. Bollström, and it was finalized together with the author of this thesis and the other co-authors.

List of other publications

- Paper 1. *Printability of functional inks on multilayer curtain coated paper*
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J. Preston, P. Salminen, R. Österbacka, J. Peltonen, M. Toivakka
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- Paper 2. *Influence of surface properties of coated papers on printed electronics*
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- Paper 3. *Low-cost hydrogen sulfide gas sensor on paper substrates; fabrication and demonstration*
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- Paper 4. *Towards Paper Electronics – Printing Transistors on Paper in a Roll-to-Roll Process*
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- Paper 5. *Printed low-voltage organic transistors on plastics and paper*
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T. Mäkelä, J. Peltonen, M. Toivakka, and R. Österbacka
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- Paper 6. *Paper Electronics*
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Advanced Materials **23**, 1935–1961 (2011).
- Paper 7. *Controlling the turn-on-voltage in low-voltage Al₂O₃ organic transistors with mixed self-assembled monolayers*
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- Paper 8. *Ferromagnetism in indium tin-oxide (ITO) electrodes at room temperature*
H. S. Majumdar, S. Majumdar, D. Tobjörk and R. Österbacka
Synthetic Metals **160**, 303–306 (2010).
- Paper 9. *Towards printed magnetic sensors based on organic diodes*
S. Majumdar, H. S. Majumdar, D. Tobjörk, and R. Österbacka
Physica Status Solidi A **206**, 2198–2201 (2009).
- Paper 10. *A recyclable paper substrate suitable for printed functionality*
R. Bollström, A. Määttänen, D. Tobjörk, P. Ihalainen,
N. Kaihovirta, R. Österbacka, J. Peltonen and M. Toivakka
Proceedings of NEXT 2009, 87-94 (2009).
- Paper 11. *Microstructural Evolution during Creep of Alloy 800HT in the Temperature Range 600 °C to 1000 °C*
J. Erneman, J.-O. Nilsson, H.-O. Andréén, and D. Tobjörk
Metallurgical and Materials Transactions A **40A**, 539–550 (2009).
- Paper 12. *Roll-to-Roll Fabrication of Bulk Heterojunction Plastic Solar Cells using the Reverse Gravure Coating Technique*
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- Paper 13. *Imaging and elemental analysis of polymer/fullerene nanocomposite memory devices*
A. Laiho, J. K. Baral, H. S. Majumdar, D. Tobjörk, J. Ruokolainen,
R. Österbacka and O. Ikkala
Materials Research Society Symposium Proceedings **1071**, 1071-F04-04 (2008).
- Paper 14. *Masstillverkningsmetod för plastsolceller*
D. Tobjörk, H. Aarnio, T. Mäkelä och R. Österbacka
Reflexer **10**, 109–113 (2008).
- Paper 15. *Plasttransistorer framställda med tryckmetoder lämpliga för kontinuerlig masstillverkning*
N. J. Kaihovirta, D. Tobjörk, T. Mäkelä och R. Österbacka
Reflexer **10**, 94–98 (2008).

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1. Introduction

The transistor is the main component in most electronic circuits, where it is used for logic function, amplification and controlling pixels in electronic displays. In a transistor the current between two contacts is controlled by the voltage applied to a third contact. The most common transistor type in conventional electronics today is the metal-oxide semiconductor field-effect transistors (MOSFET). The applications are, however, limited by the inflexibility of the inorganic materials and by the relatively high price per area and of simple circuits. These issues could, nevertheless, be solved if the electronics would be made by using organic materials instead. While most plastics that we use today are electrically insulating, the possibility of fabricating flexible inexpensive polymer based transistors [1,2] was enabled by the discovery that some conjugated polymers are semiconducting and can even be made conducting [3,4].

The most common type of organic transistor is the organic field-effect transistor (OFET), which consists of source and drain contacts, a thin organic semiconducting layer, an electrically insulating layer and a gate contact. Because of the larger energetic disorder of organic semiconductors, the charge carrier mobility is often substantially lower than that of inorganic semiconductors. Much progress has been made during the last two decades concerning the organic materials and in the performance of OFETs, but most OFETs still operate at high voltages of around 10–100 V. This is not suitable for flexible electronic applications where power from batteries, solar cells or electromagnetic induction are to be used and because of the risk of electric shock and irreversible electrochemical reactions in the presence of humidity. There are, nevertheless, various approaches that can be used in order to reduce the operation voltage to below 2 V, which are further discussed in Chapter 2.

The use of organic electronics is mainly motivated by the flexibility, low cost and solution processability of many electrically insulating, semiconducting and conducting organic materials, which potentially enables low-cost manufacturing of electronic applications, such as, flexible displays, sensors and identification tags by using printing techniques [5]. However, most demonstrated OFETs are still fabricated by using slow laboratory-scale and subtractive techniques, such as photolithography and vacuum processes and often on inflexible glass and silicon substrates. Nevertheless, in order to utilize the advantages of organic electronics, extensive work is also being conducted in

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finding ways to fully print the materials and devices on low-cost flexible plastic and paper substrates. Even metals can be printed by using particle based inks, which may be required for applications where high conductivities of thin structures are required. The main printing techniques suitable for mass-fabrication of OFETs are introduced in Chapter 3.

For truly low-cost electronic applications on large areas [6,7], the use of inexpensive paper substrates has a great potential [Paper 6]. Paper is not only the cheapest and most common flexible substrate today, but also recyclable and made of renewable resources. However, while paper has several advantages over plastic films, there are actually also great challenges of using paper as a substrate for printed electronics. This is not hard to understand, since neither paper nor printing has been developed for electronics.

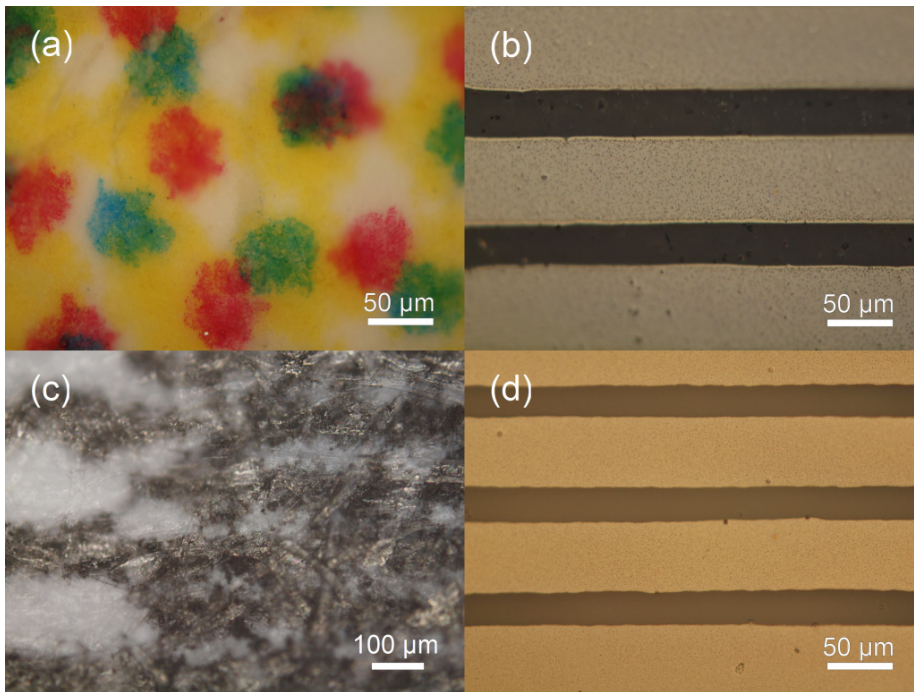


Figure 1.1. (a) An optical microscope image of the cover page of a printed magazine is shown. While it looks like a homogeneous picture at a distance, the image in fact consists of non-aligned uneven cyan, magenta and yellow dots. Images of ink-jet printed lines of a silver-nanoparticle ink are shown on (b) a polyester film, (c) a copy paper and (d) a smooth pigment coated paper.

1. Introduction

Because of the relatively low resolution of the human eye, images in magazines may actually consist of separate coloured dots, as is shown in Figure 1.1 (a). When fabricating transistors, on the other hand, the homogeneity and electronic properties of the printed structures are crucial, and high print resolution and even thin multilayer structures are required.

Examples of interdigitated structures of ink-jet printed silver nanoparticles on a plastic and two paper substrates are shown for comparison in Figure 1.1 (b–d). While the printed lines are continuous and highly conducting after heat treatment on the plastic substrate, printing of the same silver-nanoparticle ink on a copy paper results in absorption into the paper and the uneven structure (c) is still non-conducting after thermal annealing. Nevertheless, by using a paper substrate with a low surface roughness and porosity (d), it is possible to achieve similar print resolution and conductivity as on the plastic substrate.

There has recently been a great interest in the use of paper as a substrate for transistors, and different types of both organic and inorganic transistors have been demonstrated on paper [Paper 6]. This may seem like a new idea, but already in the 60's, not too long after the demonstration of the first transistor in 1948, Brody and Page at Westinghouse actually fabricated inorganic transistors on paper [8,9]. However, their approach did not have a breakthrough at that time, possibly because of the required vacuum in the fabrication process, the poor flexibility of the inorganic materials and a limited interest in such products at that time.

In the more recent demonstrations of transistors on paper, there is still typically a trade-off between the transistor performance and the printability. While high-performance conventional silicon transistors have been attached to a silicone coated paper substrate [10], screen printed silicon-nanoparticle based transistors on paper showed rather poor characteristics [11]. Gallium-indium-zinc-oxide based transistors with the paper substrate working as the electron-insulating layer [12–15] or with silicon dioxide based dielectrics [16–19] have been fabricated by using vacuum processes. Laboratory-scale techniques were also used when fabricating conventional OFETs operating at high [20–24] or low voltages [25] on paper substrates. Simple electrochemical organic transistors operating at low-voltages have been fabricated on polyethylene coated paper [26] and on photo paper [27].

Our approach of achieving printable low-voltage operating organic transistors, not only on plastics [Paper I–III], but also on paper, is to use an ion-modulated type of OFET and a smooth recyclable paper substrate with good

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barrier properties [**Paper V**]. The possibility of sintering printed metal nanoparticles on paper by applying a short exposure to a low-cost IR-lamp [**Paper IV**] makes the whole fabrication process of the low-voltage organic transistors suitable for roll-to-roll manufacturing.

Low-voltage OFETs and suitable printing techniques are introduced in Chapter 2 and 3, respectively. The experimental details are given in Chapter 4, while the results of the papers in this thesis are discussed in Chapter 5.

2. Ion-modulated organic field-effect transistors

An OFET with a top-gate bottom-contact geometry is schematically shown in Figure 2.1. OFETs are often also referred to as organic thin film transistors (OTFTs), because of the thin semiconductor layer that is used, in contrast to MOSFETs that are fabricated from a thick semiconducting substrate. The OFET structure can be considered as a parallel plate capacitor, where the gate contact and the organic semiconductor are separated by an electrically insulating layer. When a negative voltage is applied to the gate contact, electron holes (i.e. positive charge carriers) are injected from the source and drain contacts into the organic semiconductor and are accumulated by the electric field to the first few nanometres next to the dielectric interface (i.e. the channel region). OFETs that are operated in this regime are referred to as p-channel, while electrons are accumulated in the semiconductor in n-channel OFETs when positive gate voltages are applied. Considering that the conductivity (σ) is given by $\sigma = e n \mu$, where e is the elementary charge, n the charge carrier density and μ the charge carrier mobility, the rise in the charge carrier density in the channel region of the semiconductor, consequently, results in a proportionally large increase in the conductance ($g_D = \delta I_D / \delta V_D$) between the source and drain contacts.

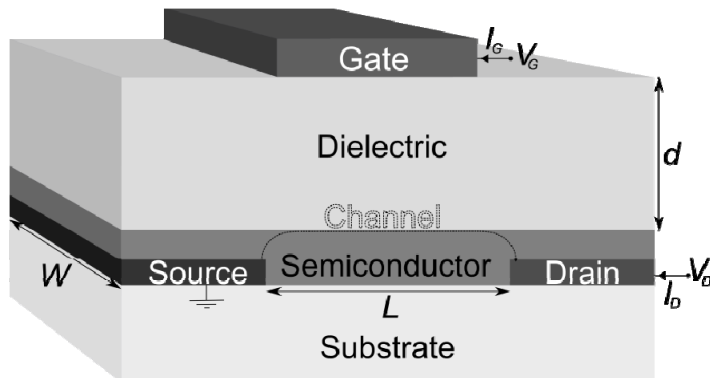


Figure 2.1. The structure of a top-gate staggered FET is shown. V_D and V_G are the voltages applied to the drain and gate contacts, respectively, while I_D and I_G are the currents. The channel length (L) and width (W) and the thickness of the dielectric layer (d) are also indicated, as well as the channel region where most of the charge transport in the semiconductor takes place.

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The charge carrier mobility of printable polymeric semiconductors ($\mu \approx 10^{-3}$ – 10^{-1} cm²/Vs) is, typically, substantially lower than that of e.g. silicon (1 – 10^4 cm²/Vs). In order to compensate for the lower mobility of organic semiconductors, a high charge carrier concentration is typically achieved by applying high voltages to the OFETs, which is unsuitable for most of the applications of organic electronics. The charge carrier concentration in the semiconductor channel is, however, not only proportional to the gate voltage, but also to the geometric capacitance (C_i) between the gate and the semiconductor. A reduced operation voltage of OFETs can therefore be achieved by increasing the capacitance across the dielectric layer. The capacitance per unit area is given by Equation 2.1, where ϵ_r is the static relative permittivity (also referred to as the dielectric constant) of the dielectrics material and ϵ_0 is the vacuum permittivity.

$$C_i = \frac{\epsilon_r \epsilon_0}{d} \quad (2.1)$$

Consequently, a large geometric capacitance can be achieved by having a low thickness of the dielectric layer ($d \ll 100$ nm) and/or by using an insulating material with a high permittivity. It is, however, hard to fabricate thin insulator layers without having problems with gate leakage currents or electrical breakthrough, and the dielectric constant of organic materials is rather low. The use of high permittivity inorganic dielectrics, on the other hand, results in low charge carrier mobility in the semiconductor, because of the randomly oriented dipoles in the gate dielectric causing a broadening of the density of states in the semiconductor close to the interface [28]. Nevertheless, by using a dielectric consisting of both alumina and a self assembled monolayer, OFETs operating at low voltages with a relatively good performance have been demonstrated [25,29–31, Paper 7]. The printability of this kind of dielectric layers is, however, poor.

An alternative way of achieving low-voltage operation is to modulate the transistors by using ions. The simplest type of an ion-modulated transistor is the electrochemical transistor [1,26,27,32,33] that may even have a lateral geometry consisting of only a conducting polymer and an electrolyte. In this kind of transistor the channel region is the area of the conducting polymer between the source and drain that is in contact with the electrolyte and can be electrochemically doped. Since the redox-reaction takes place through the bulk of the conducting polymer film, the operation is typically rather slow. Most

2. Ion-modulated organic field-effect transistors

electrochemical transistors are normally-on devices, which further limits the applications.

Another type of ion-modulated transistor is an ion-modulated OFET in which the ions are able to migrate and diffuse within the electron-insulating layer of the FET-structure, but preferably not inside the organic semiconductor layer. High capacitance and low-voltage operation are achieved thanks to the electric double layers that are formed at the interfaces of the gate dielectric. These kinds of transistors are sometimes also called electrolyte-gated or electric-double-layer (capacitance) OFETs. Various electrolytes have been used, such as, ionic liquids [34–37], ion gels [38–48], solid polymer electrolytes [49–61], polyelectrolytes [62–69], ion-conducting membranes [70,71], solutions [72,73] and water [74].

The main difference between conventional OFETs and ion-modulated ones can be understood by considering the electric field between the gate and the semiconductor. The electric field distribution within the electron-insulating layers based on a conventional dielectric material and two kinds of electrolytes is schematically shown in Figure 2.2.

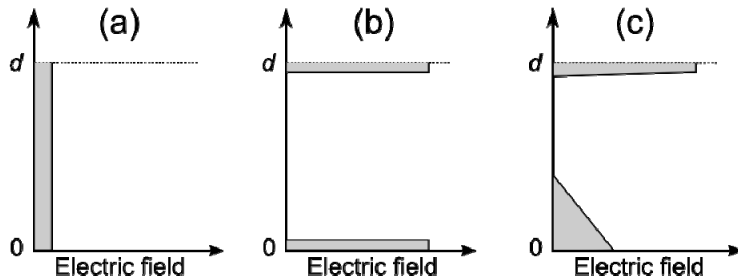


Figure 2.2. The electric field distribution inside the gate dielectric in a *p*-channel OFET when a negative potential has been applied to the gate contact is schematically illustrated for the situations of (a) a conventional dielectric, (b) an electrolyte with small ions that have formed electric double layers at the interfaces and (c) a polyanionic polyelectrolyte where the small cations have migrated to the negatively charged gate contact (top) and the immobile polyanions form a more diffuse electric double layer close to the semiconductor interface (bottom). During the formation of the electric double layers at the interfaces of an electrolyte, the electric fields will gradually change from the situation of the conventional dielectric (a) to the final situations described in (b) and (c).

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After redistribution of the ions within the electrolyte layer (and charge injection into the semiconductor channel region from the source and drain contacts), basically the whole potential difference drops across the two electric double layers at the interfaces. Because of the more bulky and immobile polyanions, the electric double layer that is formed close to the semiconductor interface is more diffuse (i.e. thicker) than when using a liquid electrolyte with smaller anions, which results in a somewhat lower capacitance. However, polyelectrolyte layers with capacitance values of above $10 \mu\text{F}/\text{cm}^2$ can still be measured at relatively high humidity levels [62].

The static capacitance is insensitive to the thickness of the electrolyte layer [75,76], which is an advantage when it comes to printing the transistors. However, when switching of ion-modulated OFETs is limited by the migration of ions within the gate dielectric, the switching time will be proportional to the thickness of the electrolyte layer [75]. As in conventional OFETs the switching speed may also be limited by the channel length, the charge carrier mobility of the semiconductor and the applied voltage ($\tau \approx L^2/\mu V$). Relatively fast switching, of below $100 \mu\text{s}$ [65,77], has been demonstrated in ion-modulated OFETs with a thin polyelectrolyte layer, a short channel length and a small parasitic electrode overlap, and even 5 GHz operation frequency has been reported with an ion-gel based gate dielectric in a more questionable demonstration [78].

In ion-modulated OFETs the penetration of ions into the bulk of the semiconductor film that is utilized in electrochemical transistors is typically unwanted, since it causes morphological changes in the semiconductor and reduces the switching performance and the charge carrier mobility. Electrochemistry can be suppressed by reducing the voltages applied below the threshold voltage for electrochemical doping and by using a polyanionic electrolyte as the gate dielectric in p-channel OFETs. Electrochemical mixing of a polyelectrolyte and a polymer semiconductor has, however, been observed when the applied gate voltage was high enough ($>1.8 \text{ V}$) to induce a charge density of above $10^{14} / \text{cm}^2$ in the electrostatic double layer [67].

We have been working with a hygroscopic insulator OFET (HIFET), which was one of the first demonstrated ion-modulated OFETs [75,79,80]. Ion-modulation takes place at normal room humidity thanks to the hygroscopicity and the dissociation of the hydroxyl groups in the weak polyacid ($\text{pK}_a \approx 10$) poly(4-vinylphenol) (PVP) that was used as the gate dielectric [75]. Because of the operation principle, the HIFET has been proposed, e.g., for sensing applications [81,82]. The applications of the HIFET are, however, limited by the

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relatively slow switching speed (<1 Hz) and low ratio of the on and off currents ($<10^3$) that is caused by the ionic charging and leakage currents and by the doping of the semiconductor. Except for this, and the low-voltage operation, the characteristics of a HIFET are rather similar to that of conventional OFETs. The typical output and transfer characteristics of a HIFET are shown in Figure 2.3.

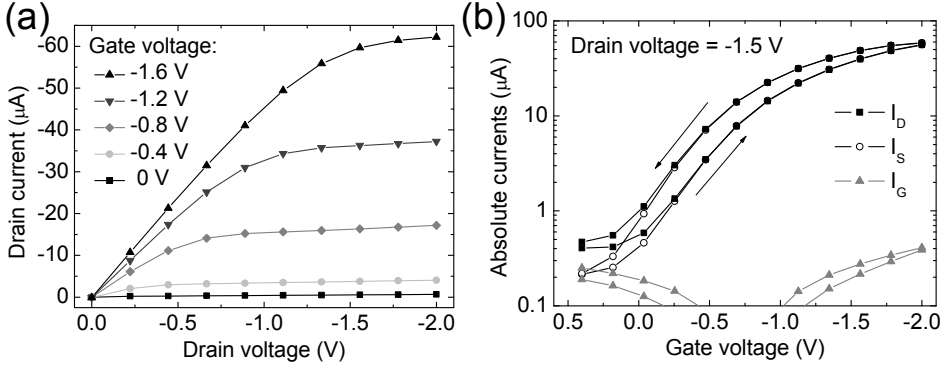


Figure 2.3. The (a) output and (b) transfer characteristics of a HIFET fabricated on a glass substrate are shown. The gate voltage (V_G) applied is indicated for each output curve. The transfer characteristics measured in the saturation regime ($V_D = -1.5$ V) are shown with a logarithmic scale of the current. The source and gate currents (I_S and I_G) are plotted together with the drain current (I_D) for comparison, and the hysteresis of the measurement is revealed by the dual sweep.

The output characteristics of a FET are obtained by sweeping the applied drain voltage at different gate voltages and measuring the drain currents. First a linear increase in the drain current is seen, but at higher drain voltages ($|V_D| > |V_G|$) the pinch-off is reached at which the current starts to saturate. This saturation regime, in which the drain current is relatively constant, is caused by the growing depletion zone in the channel close to the negative drain electrode, which limits further current rise with increasing drain voltage. When measuring the transfer curve, the drain current is measured as a function of the gate voltage, while the drain voltage is kept constant. From the transfer characteristics, parameters, such as, the threshold voltage, turn-on voltage, on/off-ratio, sub-threshold slope (S), charge carrier mobility and transconductance ($g_m = \delta I_D / \delta V_G$) can be extracted.

The analytical expression for the current between the source and drain contacts of an ideal FET is given by Equation 2.2. The current in the saturation

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regime ($|V_D| > |V_G - V_T|$) is obtained by inserting that $V_D = V_G - V_T$, which results in Equation 2.3. Among the approximations used when obtaining these equations are neglecting of the contact resistance, the diffusion of charge carriers, the conduction through the bulk of the semiconductor layer and the dependence of the charge carrier mobility on the charge carrier concentration and the electric field. The electric field along the channel is also assumed to be much lower than the transverse field generated by the gate contact. Furthermore, because of this gradual channel approximation, short-channel effects, such the lack of saturation and large off-currents that are seen when the channel length is very small, have not been taken into account. By adding a few extra parameters, the current-voltage equations can be extended to also include these kinds of effects [83].

$$I_D = C_i \mu \frac{W}{L} \left((V_G - V_T) V_D - \frac{V_D^2}{2} \right) \quad (2.2)$$

$$I_D = C_i \mu \frac{W}{2L} (V_G - V_T)^2 \quad (2.3)$$

The threshold voltage parameter (V_T) originates from MOSFET theory, where it is defined as the gate voltage at which an inversion layer is formed in the doped semiconductor at the interface to the gate dielectric. Since OFETs only operate in the accumulation regime, the threshold voltage does not have that clear physical interpretation [84], but is anyway often used as a fitting parameter. In OFETs the threshold voltage depends on the built in electric field between the gate contact and the organic semiconductor (i.e. the difference between the work function of the gate contact and the ionization potential of the semiconductor). A related fitting parameter with a more practical importance is the turn-on voltage (V_0), which is extracted from the transfer characteristics in the semi-logarithmic plot as the gate voltage at which the drain current starts to increase above the noise level or the level of the leakage currents.

The charge carrier mobility in the saturation regime can be extracted, e.g. by using Equation 2.3, from the slope of the square root of the drain current in the transfer characteristics if the geometrical capacitance and the channel dimensions are known, while the threshold voltage is obtained as the extrapolated intersection with the V_G -axis. The capacitance of an ion-modulated OFET (of up to 1–100 $\mu\text{F}/\text{cm}^2$) is, however, strongly frequency and humidity dependent [77,85] and it is challenging to correctly measure the capacitance at a

2. Ion-modulated organic field-effect transistors

frequency that corresponds to the rate of the transistor measurement. If the lower capacitance values measured at higher frequencies are used or if electrochemical doping is taking place, the calculated mobility is easily overestimated [Paper 6,79]. Exceptionally large charge carrier mobility values (of up to $4 \text{ cm}^2/\text{Vs}$) have been reported in ion-modulated OFETs based on ion gels [38– 40,43–45,48] and polymer electrolytes [57,60], but are most probably explained by bulk doping in the bulk of the polymer semiconductor. The charge carrier mobility values estimated for ion-modulated OFETs based on polyelectrolytes (where electrochemistry is suppressed) are typically much more modest ($\mu \approx 0.01 \text{ cm}^2/\text{Vs}$). Relatively large transistor currents can still be obtained (see Figure 2.3) by using printed interdigitated source and drain contacts with a large channel width-to-length ratio.

The extraction of the field-effect mobility and the threshold and turn-on voltages are often complicated by the hysteresis in the transfer characteristics. The hysteresis seen in the transfer curve of the HIFET (Figure 2.3), with higher currents in the backward sweep, is mainly caused by the relatively slow ionic drift within the gate dielectric when building up the diffuse electric double layer, but could partly also be caused by charge trapping or electrochemical effects at higher voltages. Large hysteresis in the transfer curves is especially seen when measuring a HIFET with a thick PVP layer at a low humidity level (<30 %) and at high sweep rates to high voltages.

Another factor affecting the transistor performance, in addition to the ion-modulation and the charge transport through the semiconductor channel, is the charge injection into the semiconductor at the source and drain contacts [86]. If the work function of the source and drain contacts is far from the ionization potential of the semiconductor (in a p-channel OFET), this could result in a large contact resistance and diode-like current voltage dependence. The contact resistance is also affected by the FET-geometry. In an OFET with coplanar geometry (i.e. top-gate top-contact or bottom-gate bottom-contact) the charges are injected at the edge of the source and drain contacts into the semiconductor channel, while in a staggered configuration (see the top-gate bottom-contact geometry in Figure 2.1) the charges are injected into the semiconductor over a larger area, which typically results in a lower contact resistance. In a staggered OFET the charges must, on the other hand, travel through the undoped bulk of the semiconductor before reaching the channel, which may contribute to the contact resistance.

2. Ion-modulated organic field-effect transistors

In order to fabricate complementary circuits [87], n-channel OFETs are required in addition to p-channel OFETs. However, most polymer semiconductors provide a higher mobility of holes than of electrons, and the electron conduction is also often degraded in air and inhibited by hydroxyl groups at the interface of the semiconductor [88]. There have, nevertheless, recently been improvements in both the stability and electron mobility of organic semiconductors [89–91], and even n-channel ion-modulated OFETs have been demonstrated [36,37,47,68,69]. However, when preventing bulk doping of the semiconductor in n-channel ion-modulated OFETs, a polycationic instead of a polyanionic material should be used as the electron-insulating material [68,69].

3. Printing techniques

3.1. Traditional printing techniques

Flexography, gravure, offset and screen printing have a relatively long history, but are still among the main printing techniques used. The most fundamental differences between these techniques can be realized by comparing the schematic structure of the printing plates shown in Figure 3.1.

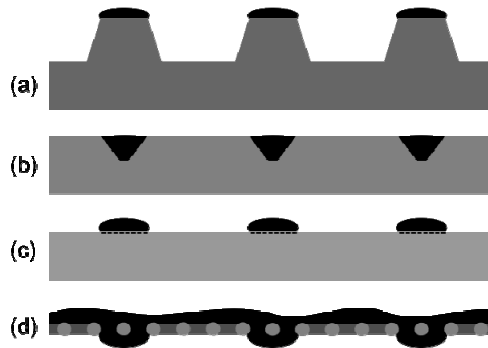


Figure 3.1. Cross sections of the printing plates used in the conventional printing techniques (a) flexography, (b) gravure, (c) offset and (d) screen printing are schematically shown. The printing ink that is to be transferred to the substrate is black.

In flexographic (flexo) printing, the patterns that are to be printed onto a substrate are raised on the flexible printing plate, while the patterns are engraved into the metal plate that is used in gravure printing. In gravure printing the whole gravure plate is first inked, after which the excess ink next to the etched cells is removed by using a doctor blade. The raised patterns on the flexo plate are usually inked by using an anilox roll that consists of a homogeneous pattern of engraved cells on a ceramic surface. The thickness of the printed structures in gravure and flexo printing depends on the depth of the cells of the gravure plate and of the anilox roll, respectively. In offset (lithography) printing both the printing and non-printing areas are roughly at the same level on the printing plate, but the method is instead based on a difference in the surface energy. In screen printing the printing “plate” consists of a mesh where the holes of the non-printing areas are blocked, and the ink is pushed through the open pores of the stencil screen onto the substrate when a rubber blade (squeegee) is moved across the surface. Screen printing is quite commonly used as a flat printing

3. Printing techniques

technique in batch processes, while flexo, gravure and offset printing are mainly used for high volume production in continuous roll-to-roll processes, in which case the printing structures are formed on a cylinder instead of a plate.

In gravure printing a relatively high print resolution can be achieved, and a rather low viscosity of the ink can be used of around 50–100 mPas. However, the high price of the engraved metal rolls makes the technique mainly suitable for very long print runs of the same patterns. Additional restrictions may arise from the high print pressure used in conventional roll-to-roll systems, as well as the challenges with unprinted dots on substrates with a high surface roughness. The flexo plates, on the other hand, are inexpensive, but the main limitations of flexo printing are poor solvent compatibility of the flexible plate, relatively low print resolution and the halo effect when the ink is squeezed outside the printing areas due to the print pressure. Offset printing is a very common technique in the graphics industry, and enables relatively high print resolution. However, the use of this technique for printing electronics is limited by the high required viscosity of the ink of around 5–200 Pas, the relatively high print pressure and the typical presence of water. Thick layers can be deposited by screen printing, but the print resolution is low. Rather high ink viscosity is typically also required, but the properties and ink requirements strongly depend on the mesh that is used.

One of the challenges for printing electronics is the use of discrete cells of the gravure (and anilox) rolls, which typically also results in discrete patterns on the substrate. Continuous print patterns can, however, be achieved by using continuous lines and a small ratio of cell spacing to cell width. Optimizing the print pressure of the flexo roll and using a relatively low viscosity low surface tension ink that merges on the substrate [92,93] is also useful when printing continuous structures.

Flexo printing [94–101], as well as gravure printing [98–109], has recently been used in the fabrication of OFETs operating at high voltages (10–100 V). Offset printing has mainly been used for applying metal and conducting polymer structures [95,110,111]. Screen printing has been used for applying some of the layers of OFETs [104,112,113], and all the layers of a silicon-particle based FET [11]. Fully printed OFETs operating at high voltages have been demonstrated by the groups of Hübler [95,96,99–102] and Cho and Subramanian [103,106–109], while we have even demonstrated fully printed low-voltage OFETs [**Paper II**]. In addition to this, there are several examples of fully ink-jet and aerosol-jet printed transistors shown in the following section.

3.2. Ink-jet printing

Ink-jet printing is a low-cost non-contact printing technique that produces digital patterns at a relatively high resolution and with low material consumption. The printing technique is nowadays widely used in homes for printing documents from the computer, but has recently also gained a growing interest as a method for printing various functional materials and in the fabrication of transistors, mainly because of the low ink viscosity requirement, low ink consumption, low cost and simplicity of changing the digital print patterns [114,115]. While the throughput is relatively low, the technique is compatible with a roll-to-roll process. Furthermore, when printing the top layers of organic transistors a non-contact printing technique could be advantageous, because of the reduced risk of destroying the previously printed layers if the solvents are properly chosen not to dissolve the previous layers.

There are two main types of ink-jet printers; continuous and drop-on-demand. In the continuous ink-jet printers a continuous stream of droplets are deflected towards the substrate or for recycling by an electric field. This system, which is relatively similar to a patented idea by Lord Kelvin from 1867, is mainly used for high throughput printing. In the two main types of drop-on-demand printheads droplets are ejected from the small nozzles (10–100 μm) when a pressure pulse is created by a piezoelectric- or thermoelement, as is schematically shown in Figure 3.2.

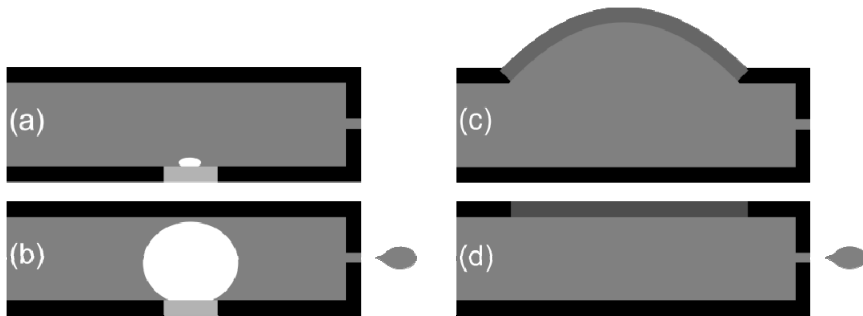


Figure 3.2. The images schematically illustrate the production of droplet from the (a–b) thermal and (c–d) piezoelectric drop-on-demand printheads. Droplets are ejected due to the increase in the pressure that is caused by the vapour bubble formation at the heating element in the thermoelement in (a–b) and by the motion of the piezoelectric material in (c–d) when applying an electric field.

3. Printing techniques

Thermal printheads are less expensive than piezoelectric ones, and are the most common ones in consumer ink-jet printers. However, the vapour bubble formation in the thermal method is mainly suitable for water based inks that are not heat sensitive, or aggregates inside the nozzles. This is why most ink-jet printing in the industry and of functional materials is done using piezoelectric printheads, but conducting polymers have also been printed by using thermal printheads [116]. Most polymeric semiconductors have a relatively low solubility, which is rather suitable for ink-jet printing that, in contrast to the traditional printing techniques, only works with low-viscosity inks.

A common problem of ink-jet printing is clogging of the nozzles, especially when using small nozzle sizes and particle-containing inks. Even partial clogging can be problematic causing satellite drops or misplaced drops. This kind of trouble can be prevented by proper tuning of the ink properties to a low viscosity (<10–40 mPas), suitable surface tension and low evaporation rate (i.e. high boiling point solvents). In order to print particle based inks, it is important to use stable dispersions of particles that are much smaller than the nozzles (<1/100).

Uneven drying of the printed structures is commonly seen when low-viscosity inks are used on non-absorbing substrates. The frequently observed “coffee-stain effect” with more dried material close to the edges is caused by the outward convective flow within the deposited ink compensating the faster evaporation of the solvent at the edges of the printed structures [117]. This effect is not desired when printing organic transistors that require homogeneous structures with a constant thickness. More even drying can be achieved by preventing pinning of the contact line, using an ink with high viscosity and particle concentration, changing the solvent evaporation rate, printing very small structures [118], or changing the shape of the particles [119]. Another way of avoiding the coffee-stain effect is to mix a high-boiling-point low-surface-tension solvent with a low-boiling-point high-surface-tension solvent, which may compensate the outward flow with the inward Marangoni flow that is created by the surface tension gradient [120,121,122]. In order to achieve structures with high print resolution and suitable thickness and without any bulging or scalloping effects, proper tuning of the printing parameters, such as drop spacing, jetting frequency and temperature, is also required [123].

Although ink-jet printing is roll-to-roll compatible, the printing speed is typically lower than in offset, gravure and flexo printing, especially when the printed ink evaporates slowly or when small nozzles are used in order to achieve

3. Printing techniques

higher print resolution. Narrow structures of down to 1 μm have been demonstrated by using laboratory scale ink-jet printing systems based on a very small nozzle size and electrical charging of the ink [124,125].

A digital printing technique that is almost as common as ink-jet printing is laser printing, which is based on a xerographic printing process similar to that in most photocopiers. However, the use of materials for electronics is limited by the requirements of the dry ink (toner) and by the fusing temperatures of up to 200 °C. Among the less common digital printing techniques are aerosol-jet printing, liquid dispensing, omnidirectional printing [126] and organic vapour-jet printing [127,128]. However, the printing speed of the last methods may be very limited.

Aerosol-jet printing, which is rather similar to ink-jet printing, has actually been used for fabricating fully printed electrolyte gated OFETs [39,46,78]. There are also demonstrations of more or less fully ink-jet printed transistors [27,129–135], but in most examples ink-jet printing has been used for depositing only some of the transistor layers and in combination with laboratory scale techniques [136–141]. In the work presented in this thesis ink-jet printing was mainly used for applying the transistor contacts and the semiconductor layer of low-voltage organic transistors.

The typical range of ink viscosity and thickness and print speed and resolution of ink-jet printing is compared to that of the traditional printing techniques in Table 1. The estimated lateral print resolution of the different techniques is shown in micrometers, but the smallest line width, line separation and registration may vary strongly, and higher print resolution have been achieved in low-throughput laboratory-scale printing systems [124,125]. Among the challenges of using the traditional contact printing techniques for fabricating organic transistors is the typically relatively high ink viscosity required (0.05–100 Pas), which is not suitable for solution processable electronic materials that have a limited solubility. Lower ink viscosities (of down to 1–10 mPas) than listed in the table have, nevertheless, been used when gravure and screen printing polymeric semiconductor solutions [102–105].

3. Printing techniques

Table 1. Typical processing parameters used in the most common printing techniques [Paper 6,102,142].

| Printing technique | Ink viscosity [mPas] | Wet film thickness [μm] | Print speed [m/min] | Print resolution [μm] |
|--------------------|----------------------|--------------------------------------|---------------------|------------------------------------|
| Ink-jet | 1–40 | 0.3–20 | 1–100 | 20–50 |
| Flexo | 50–500 | 0.5–8 | 50–500 | 30–75 |
| Gravure | 50–200 | 0.1–5 | 20–1000 | 20–75 |
| Offset | 20 000–100 000 | 0.5–2 | 15–1000 | 20–50 |
| Screen | 100–50 000 | 3–100 | 10–100 | 50–100 |

3.3. Other techniques

Because of the challenges of using conventional printing techniques for fabricating transistors, several types of laboratory scale “printing” techniques have been used, such as, microcontact and transfer printing (that are rather similar to flexo printing) and micromolding in capillaries [143,144]. While high print resolution can be achieved, these laboratory techniques typically involve several time consuming steps and are incompatible with a fast roll-to-roll process.

Coating techniques can be used for applying layers that do not need to be patterned or when the requirements on the lateral resolution are low. The laboratory scale spin coating technique is commonly used for applying the semiconducting and insulating layers of OFETs. There are, however, other coating techniques that can be used in a roll-to-roll process, such as, slot-die, curtain, knife-over-edge, air knife, metering rod, dip, gravure, reverse gravure and spray coating. Many of these techniques have been used, e.g., for fabricating organic solar cells [Paper 12, Paper 14, 145–147]. A vapour deposition system is also compatible with a roll-to-roll process, but the required vacuum makes the process expensive. When fabricating transistors we have especially used the reverse gravure coating technique, since it enables coating of homogeneous layers and with better control of the thickness than by the conventional printing techniques.

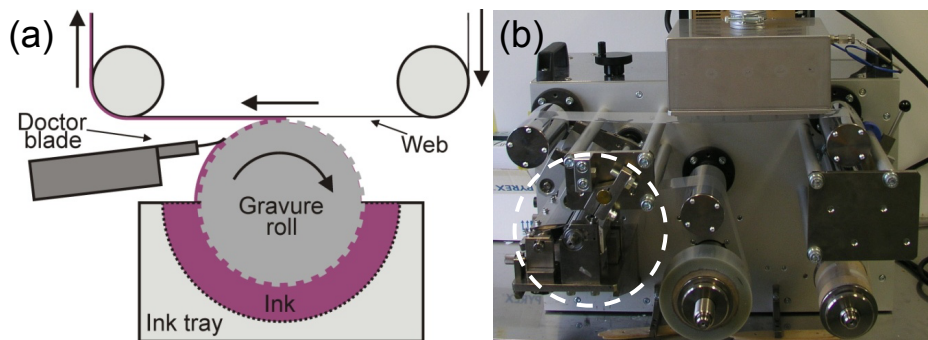


Figure 3.3. (a) A schematic image and (b) a photo of the reverse gravure coating technique are shown. The photograph shows the whole coating machine, including the unwinding and rewinding rolls and the air dryer. The part where the actual coating takes place is situated within the area indicated by the dashed circle.

The reverse gravure coating technique cannot be used for high resolution patterning, but has the advantage of producing thin homogeneous layers with a controllable thickness for a wide range of ink viscosities (1–2000 mPas). In reverse gravure coating the gravure roll is rotating in the opposite direction as the web, which gives a more stable coating at higher coating speeds than in the forward mode and than by plain roll coating. The reverse gravure coating process is schematically shown in Figure 3.3 together with a photo of the Mini-Labo test coater (Yasui Seiki Co.) that was used in this work. The metal gravure roll consisting of engraved tri-helical grooves is covered with ink when it rotates through the ink tray. The excess ink is then removed by the trailing flexible metal doctor blade, leaving ink only inside the engravings. As the web passes the roll in the opposite direction for a short distance, a fraction of the ink is transferred to the web and forms a smooth layer. A dryer with controllable air flow and temperature can be used in order to completely evaporate the solvent before the web is rewound.

The dry thickness of the coated layer can be varied mainly by changing the ink concentration, the volume of the engravings and the web to roll speed ratio [Paper I, 148–150]. Although the print pressure is very low (“kiss-contact”), since no backing roll is used, care must still be taken that the solvents used do not dissolve the previously deposited layers. The reverse gravure coating technique was used in **Paper I**, **Paper II** and **Paper III** for subsequently applying the thin semiconductor and the more than 50 times thicker electronic insulating layer of the HIFET.

4. Experimental

4.1. Materials

The substrates and different types of materials that we have used for fabricating low-voltage organic transistors are described in this section. An OFET consists of materials with different electrical properties; conducting, semiconducting and insulating. Since all materials should be inexpensive, flexible and printable, we have mainly used solution processable polymer based materials. A silver ink was, however, used when printing the source and drain contacts, because of the requirements of a high and stable conductivity and high print resolution. The semiconductor should be air stable, form a thin and homogeneous layer, have a high charge carrier mobility and make an Ohmic contact to the source and drain contacts (i.e. ionization potential close to the work function of the source and drain material). The dielectric layer should be homogeneous, electrically insulating and have a high capacitance. All layers should also be applied without dissolving or degrading the previous ones.

4.1.1. Substrate

Low-cost flexible plastic and paper substrates have been used for fabricating the transistors in this thesis. Two different commercial polyester substrates were used; Melinex 505 and Mylar A (DuPont Teijin Films). The root mean square (RMS) surface roughness of the 50 μm thick and 12 cm wide Mylar A film on a roll was around 25–50 nm, while it was only 4–6 nm on the 100 μm thick Melinex 505 sheets (see **Paper III**). The plastic substrates were cleaned with de-ionized water, acetone and isopropanol before use. Cut microscopy glass slides were used as a rigid support when applying the polymer solutions by spin coating (in **Paper I**, **Paper III** and **Paper V**). Glass slides were also used as reference substrate in **Paper IV** after depositing a self assembled monolayer of hexamethyldisilazane.

The recyclable multilayer coated paper substrates used in **Paper IV** and **Paper V** were developed in laboratory scale for having good barrier properties and a low surface roughness and porosity. A 10 cm wide base paper pre-coated with coarse ground calcium carbonate (100 g/m^2) was first blade-coated with a 10 g/m^2 kaolin layer in order to reduce the surface roughness from 600 nm to 300 nm. A barrier layer (0.5–40 g/m^2) consisting of ethylene acrylic acid copolymer latex (Tecseal, Trüb Emulsions Chemie AG) blended with high aspect

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ratio platy mineral pigments was then coated on the smoothing layer. The thin (3–7 g/m²) top layer was reverse gravure coated by using a dispersion of kaolin (Ultrafine Platy, Imerys Ltd.) in water and isopropanol that was blended with up to 12 wt.% of a styrene butadiene latex binder (DL 920, Styron Europe GmbH) and 2.5 wt.% of carboxy methyl cellulose (Finnfix 5, Noviant Oy). A relatively low RMS surface roughness of 55–75 nm was measured by AFM after calendering. The commercial papers Lumiart 150 (StoraEnso), Glossy and Matte photo paper (Canon) and copy paper (80 g/m²) were used as reference substrates.

4.1.2. Contacts

In all the transistors described in this thesis, the source and drain consisted of silver or gold, while the gate contacts were based on the polyelectrolyte complex of the hole-conducting polymer poly(3,4-ethylene dioxythiophene) with poly(styrene sulfonate) as the counter-ion (PEDOT:PSS). The use of metals for the source and drain contacts was motivated by the requirement of a relatively low resistance, especially when printing thin interdigitated finger structures and circuits. For the gate contacts, on the other hand, a larger resistance was allowed and PEDOT:PSS was used, because the water based dispersion could be applied by drop casting or ink-jet printing without causing an electrical shortage to the source and drain contacts by dissolving the underlying non-crosslinked PVP layer.

Two commercial dispersions of polymer capped silver-nanoparticles were used (AG-IJ-G-100-S1, Cabot Corp. and SunTronic Jettable Silver U5603, Sun Chemicals Corp.) and worked almost equally well for ink-jet printing the source and drain contacts. The inks consisted of around 30–50 nm large polymer dispersed silver nanoparticles (20 wt.%) in the solvents ethanol and ethylene glycol, and had a viscosity of 10–15 mPas and a surface tension of 27–31 mN/m. In order to obtain a low resistivity of the printed structures, thermal annealing of the printed silver nanoparticles on plastic substrates was carried out on a hot plate or in an oven at 120–130 °C for 20–30 min. On paper substrates (in **Paper IV** and **Paper V**) high conducting structures were achieved by irradiation from an IR-lamp for 10–15 s. In **Paper IV** dodecanethiol and butanethiol protected gold-nanoparticles were also used for ink-jet printing after dispersing them in p-xylene. Furthermore, a thermally evaporated 100 nm thick silver film was used in **Paper IV**, and in **Paper I** and **Paper III** 30 nm thick gold source and drain contacts ($L \approx 35 \mu\text{m}$, $W \approx 1.5 \text{ mm}$) were thermally evaporated through a

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shadow mask. For flexo printing a commercial silver flake based ink (125-06, Creative Materials Corp.) was used after diluting with 1-methoxy-2-propanol acetate and a carbon based ink (110-04, Creative Materials) was used after diluting with methyl ethyl ketone.

The chemical structure of PEDOT and poly(styrene sulfonic acid) (PSS:H) is shown in Figure 4.1. Commercial dispersions (Baytron P, H.C. Starck GmbH / Clevios P, Heraeus Clevios GmbH) of PEDOT:PSS gel particles in water with a ratio of 1:2.5, a solid content of 1.2–1.4 wt.%, a viscosity of 60–100 mPas and an achievable conductivity of up to 10 S/cm was used for drop casting the gate electrode. The same dispersion was also used for ink-jet printing the gate contact in **Paper I** after diluting with de-ionized water (1:1) and adding a small amount of a non-ionic surfactant (Triton X-100, Sigma-Aldrich Co.) just before printing. However, in **Paper II** and **Paper III** the gate contact was applied in two layers by first ink-jet printing the water based low-conducting (1000 Ωcm) Baytron P Jet PE FL ink (LC), which protected the PVP-layer from being dissolved when, finally, the highly conducting (30–90 S/cm) but ethanol containing Baytron P Jet HC ink (HC) was inkjetted. Clevios PH 500, which is both water based and relatively conducting, was later used for ink-jet printing in a roll-to-roll process after adding a small amount (0.1 vol.%) of Triton X-100 just before printing. The small size of the gel particles (≈ 30 nm) in this dispersion is suitable for ink-jet printing and forms high conducting structures (100–1000 S/cm) thanks to morphological changes during the drying process when adding a high boiling point solvent, such as ethylene glycol or dimethylsulfoxide. For flexo printing a relatively viscous PEDOT:PSS ink was used; either Baytron P with an increased viscosity by roto-evaporation to a concentration of about 1.7 wt.% or Clevios P HC V4 with a viscosity of 100–350 mPas.

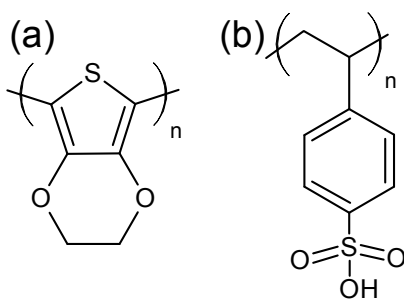


Figure 4.1. The chemical structure of (a) PEDOT and (b) PSS:H is shown.

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4.1.3. Semiconductor

In OFETs the semiconductor layer is very crucial and often limits the field-effect mobility, on/off ratio and air stability. In order to be able to print the semiconductor, the solubility of the semiconductor material is also an important parameter, which is often obtained by attaching alkyl side chains to the polymer backbone. Among the most commonly used solution processable conjugated polymer semiconductors is regioregular head-to-tail poly(3-hexylthiophene) (P3HT) that forms a polycrystalline film with lamellar structures and may have a charge carrier mobility of up to $0.2 \text{ cm}^2/\text{Vs}$ [151–152]. P3HT (Plexcore OS-1100, Plextronics Inc.) was used as the semiconductor in all the transistors in the included papers in this thesis. It is most soluble in chlorinated hydrocarbon solvents, such as, chloroform and chlorobenzenes, but also relatively soluble in tetrahydrofuran and aromatic hydrocarbon solvents, such as, toluene and xylene.

An issue when using P3HT in OFETs in ambient air is, however, the relatively large off-currents that are caused by oxygen doping [154] of the semiconductor and by the interactions with moisture [155]. Better stability towards oxidative doping can be achieved by using a semiconductor with a slightly higher ($\approx 0.1 \text{ eV}$) ionization potential, such as poly(3,3'-didodecyl-quarterthiophene) (PQT-12) [137,156,157]. The chemical structure of the two polythiophenes is shown in Figure 4.2. The solubility of PQT-12 is lower than that of P3HT, but, except for the charge carrier mobility, the overall transistor performance was typically better when using PQT-12 (ADS12PQT, American Dye Source).

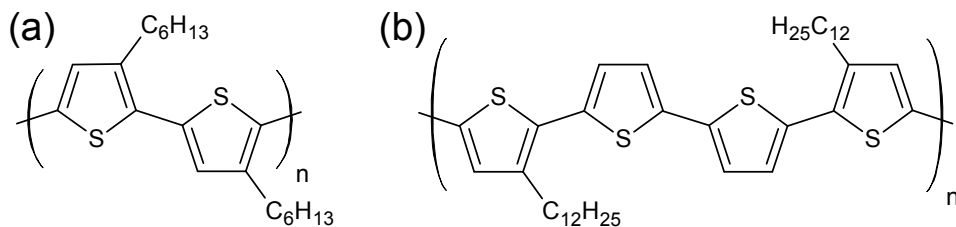


Figure 4.2. The chemical structure of (a) P3HT and (b) PQT-12 is shown.

Among the challenges when applying the semiconductor layer was to achieve a homogeneous layer with a proper thickness of around 20–50 nm [158] by varying the ink concentration and the coating and printing parameters. While a too thin semiconductor layer results in low transistor currents, a too thick

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semiconductor layer, on the other hand, results in large off currents in the case of P3HT, and a large contact resistance in the case of PQT-12.

Low concentration P3HT and PQT-12 solutions (0.3–1 wt.%) in p-xylene, toluene, chloroform, chlorobenzene, ortho-dichlorobenzene and mesitylene were applied by spin coating, reverse gravure coating, ink-jet printing or spray coating. When spin coating the P3HT layer, best transistor performance was typically achieved by using xylene as the solvent, and by subsequently annealing the film on a hot plate at 120 °C for 20 min. Because of the lower solubility of PQT-12, mainly chlorobenzene or dichlorobenzene was used as the solvent.

4.1.4. Gate dielectric

Non-cross-linked poly(4-vinylphenol) (PVP) (P25ED, DuPont Electronic Polymers) with a molecular weight of 25 000 was used as the hygroscopic electronic insulating material in the fabricated HIFETs in this thesis. The chemical structure of PVP is shown in Figure 4.3. The PVP layer was mainly applied by spin coating and reverse gravure coating. A solution of 10 wt.% PVP in isopropanol and ethylacetate was used in **Paper I** and **Paper V** and in **Paper II** and **Paper III**, respectively.

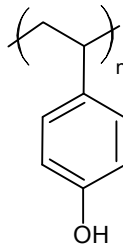


Figure 4.3. The chemical structure of PVP is shown.

The ion modulation in the HIFET takes place at normal room humidity thanks to the protons that dissociate from the phenol groups and migrate to the gate contact when a negative voltage is applied. Much of the transistor characteristics are rather insensitive to the thickness of the hygroscopic insulator layer [75], but the switching speed decreases with the PVP-thickness and increases with the relative humidity. Furthermore, it is still important that the gate dielectric is thick enough in order to prevent electrical shortage when applying the gate contact, but not so thick that cracks will form during the drying process. For this reason a PVP thickness of around 1–2 μm was used in this work.

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4.2. Printing

4.2.1. Inkjetting

A photo of the tabletop piezoelectric drop-on-demand ink-jet printer (Dimatix Materials Printer, DMP-2831, FUJIFILM Dimatix Inc.) that was used for fabricating the transistors is shown in Figure 4.4. The ink-jet printer was used for applying the gate contacts [Paper I–III], source and drain contacts [Paper II–V] and the semiconductor [Paper 6].

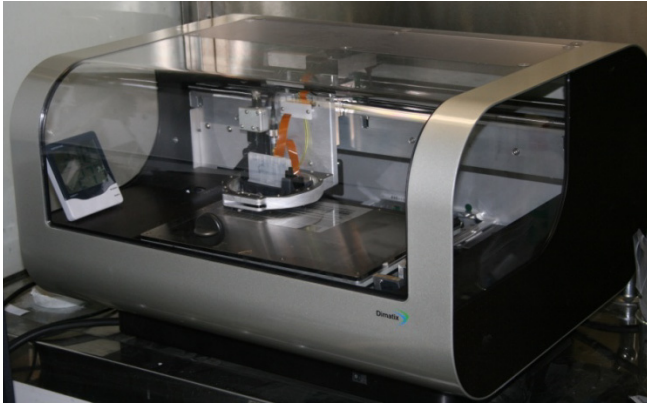


Figure 4.4. A photograph of the tabletop ink-jet printer used for fabricating transistors. The cartridge moves sideways, while the vacuum platen is stepped towards the back during printing.

All inks were filtered through 0.45 μm filters made of polytetrafluoroethylene or polypropylene before filling the 1.5 ml large ink-jet cartridge (DMC-11610) that consists of 16 piezoelectric nozzles with a diameter of around 20 μm and produces droplets with a nominal volume of 10 pL. According to the manufacturer, the ink should have a viscosity of 10–12 mPas and a surface tension of 28–33 mN/m, but it was also possible to print inks with properties outside this range after tuning the jetting parameters. The driving voltage was around 15–25 V, the pulse width around 4–10 μs and frequency usually at 15 kHz. The print height was kept at about 1 mm and the temperature of the vacuum platen was sometimes increased in order to increase the drying speed. The print thickness was controlled by changing the drop spacing between 10 and 50 μm . The final print resolution was affected by the previous parameters, as well as by the surface energy of the substrate and the surface tension and viscosity of the ink.

4. Experimental

4.2.2. Reverse gravure coating

The reverse gravure coating technique was introduced in Section 3.3. A photograph of homogeneous P3HT-coatings of different thickness on a 12 cm wide polyester film is shown in Figure 4.5. The coating thickness was controlled by changing the web and roll speeds. The maximum web speed of the Mini-Labo test coater was 1.6 m/min, and a roll speed of up to 3 m/min (48 rpm) was possible to use. The pickout fraction was studied as a function of the coating parameters, and was calculated by multiplying the measured coating thickness (wet) with the web speed and dividing with the average depth of the engravings in the gravure roll times the roll speed. The 20 mm diameter roll having 47 grooves/cm (120 grooves/inch) with a depth of 60–70 μm was found to be suitable for coating both the semiconductor and the hygroscopic insulator solutions (in **Paper I-III**). Since the volume of the regular ink container was quite large (around 100 ml), a separately made ink tray with a volume of around 10 ml was drilled from a Teflon block and was used when coating the more expensive organic semiconducting material.



Figure 4.5. Thin (10–50 nm) and homogeneous P3HT layers applied by reverse gravure coating onto a 12 cm wide polyester film are shown.

4.2.3. Roll-to-roll hybrid printing line

An in-house built roll-to-roll based hybrid printing line, called the “Funprinter”, was used for fabricating organic transistors in different ways. A photograph of the Funprinter is shown in Figure 4.6 where some of the parts are indicated with capital letters. It is a flexible printing system in the sense that different printing and coating units can be changed into various positions and combinations. A web speed of around 2–10 m/min was used.

4. Experimental

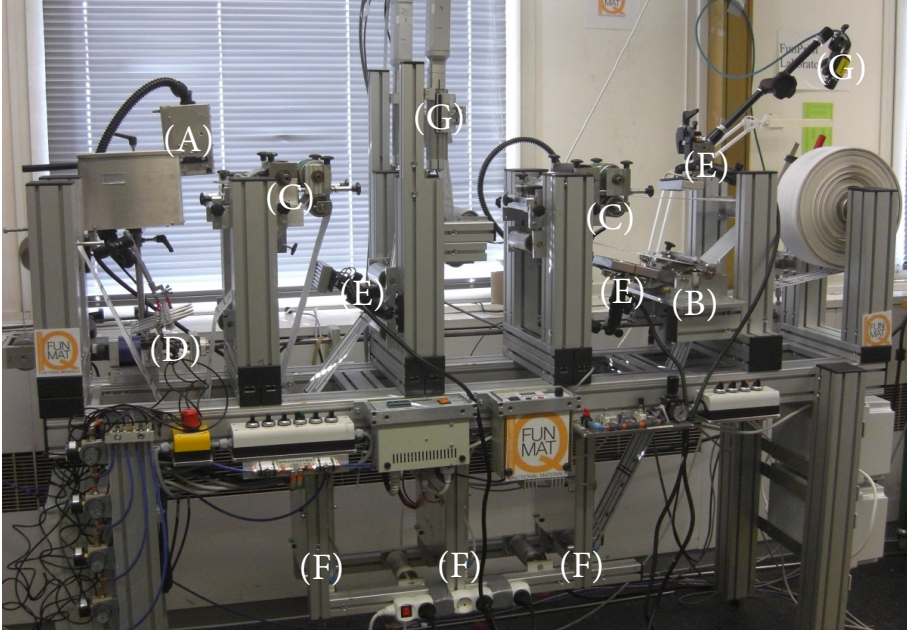


Figure 4.6. The roll-to-roll hybrid printing line is shown with capital letters marking the different units currently installed: (A) ink-jet printer, (B) reverse gravure coater, (C) 2 flexo printers, (D) 4 spray coaters, (E) 4 IR-lamps, (F) 3 ovens and (G) alignment system with camera.

In the roll-to-roll setup an ink-jet head (Xaar 128/80) consisting of 128 nozzles with a nominal drop volume of 80 pL was used together with an Imaje 4400 controller and a separate small ink feeding system. Both the organic semiconductor and the gate contact of organic transistors were applied by ink-jet printing in this roll-to-roll system [Paper 1, Paper 4]. The alignment in the print direction could be controlled via an optical sensor detecting variations in the contrast from the previously printed structures on the substrate.

The reverse gravure coating unit in the Funprinter was constructed with similar dimensions as that of the tabletop test coater, but could be operated at higher speeds. Both the semiconducting and electronic insulating layers of organic transistors could be applied in this way. Four airbrushes were also used for applying the organic semiconductor layer in the Funprinter [Paper 4]. A motivation to use spray coating for applying the polymer semiconductor layer on paper was the reduced absorption into the paper substrate because of the partial solvent evaporation from the sprayed droplets before reaching the substrate. However, it was still relatively challenging to obtain a homogeneous

4. Experimental

coating with a controlled thickness when using this relatively simple technique. The coating thickness and homogeneity was controlled by varying the web speed, spraying distance, spraying pressure and ink feed.

The flexo printing unit in the Funprinter was used for applying the contacts of organic transistors. A commercial (Shore A 69°, ASAHI DSH) photopolymer printing plate and a ceramic anilox cylinder (Cheshire Engraving Services Ltd., 69° cell angle, 120 cells/cm) with a cell volume of 12–30 cm³/m² were used. The source and drain structures on the flexible printing plate consisted of 3–12 interdigitated fingers separated by around 300 μm and with an overlapping distance of 5 or 12 mm. A halo effect was often seen around the flexo printed structures to an extent depending on the applied print pressure, the cell volume of the anilox, the viscosity of the ink and the porosity of the paper surface. This resulted in a trade-off between the print resolution and the conductivity of the printed structures. Using a silver-flake based ink, source and drain structures were flexo printed with a surface resistivity of down to 1–3 Ω/sq and with a distance between the contacts (channel length) of down to 200 μm. High printing speeds typically resulted in the best printing results, but the speed was limited by the relatively slow drying process and IR-treatment of the printed inks. PEDOT:PSS and carbon based inks were also flexo printed, but the surface resistivity was typically above 10 kΩ/sq.

In addition to the three ovens with air flow, up to eight 500 W IR-lamps (HQE 500, Ceramicx) were also used at a short distance (1–10 cm) in order to increase the drying speed and the conductivity of the printed silver structures. The IR-exposure of flexo printed interdigitated contacts is shown in Figure 4.7. When sintering the ink-jet printed silver-nanoparticle inks on paper an IR-lamp based on three 2 kW strip light bulbs (IRT systems, Hedson Technologies AB) was used at a distance of around 20 cm.

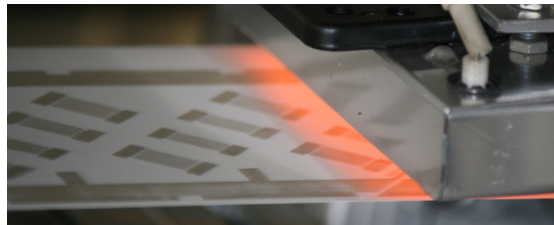


Figure 4.7. Low resistance of the flexo printed silver structures were achieved after exposing them to IR-lamps in the roll-to-roll process.

4. Experimental

4.3. Measurements

4.3.1. Electrical characterization

The electrical characterization of all transistors was done in darkness in ambient air at a relative humidity of around 25–35 % by using an Agilent 4142B modular DC source/monitor (Agilent Technologies Inc.) that was connected to a computer and controlled with programs written in LabView (National Instruments Corp.). The output and transfer characteristics were measured at a sweep rate of around 200 mV/s and 100 mV/s. Resistivity measurements of ink-jet printed conducting lines were made on a digital multimeter (Keithley 2100 USB, Keithley Instruments Inc.) using four probes in order to avoid contribution from the contact resistance.

4.3.2. Optical characterization

An optical microscope was used for studying the printed structures. The line-edge roughness (waviness) of ink-jet printed interdigitated silver contacts on plastics and paper was obtained from optical microscope images by using the software SuMMIT (EUV Technology).

In order to determine the thickness of polymer coatings on transparent plastic substrates in **Paper I-III**, the atomic force microscope (AFM) could not be used, but instead the thickness was derived from the absorption spectra of the films. The spectra were measured by using an absorption spectrophotometer (U-3200, Hitachi High-Technologies Corp.) that was connected to a computer. The typical absorption spectra (also including reflected and scattered light) of coated films of P3HT and PVP are shown in Figure 4.8.

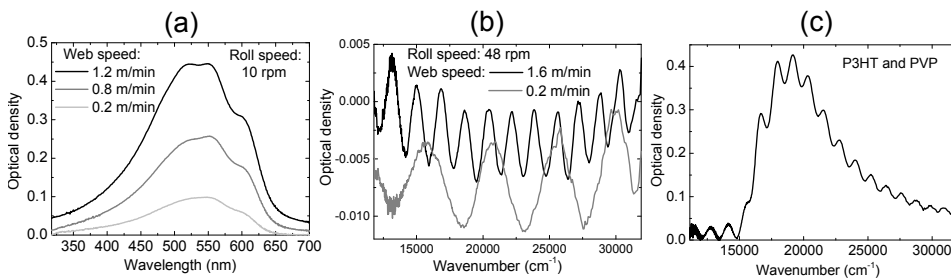


Figure 4.8. The absorption spectrum of reverse gravure coated films of (a) P3HT and (b) PVP, as well as (c) a transistor with both layers, are shown. The spectra were used in order to determine the thickness of the coated layers.

4. Experimental

The P3HT thickness was calculated by simply assuming a linear relation between the thickness and the optical density at 560 nm, and by using the absorption coefficient value ($2.5 \times 10^5 \text{ cm}^{-1}$) determined from spin coated films on glass with a known thickness (from AFM measurements). The thickness of the transparent μm -thick PVP-layer was determined from the interference in the transmission spectra (see Figure 4.8 (b)). Ignoring the wavelength dependence of the refractive index of PVP ($n \approx 1.6$), the thickness (d) can be calculated by simply extracting the difference in wavenumber ($k \equiv 1/\lambda$) between two adjacent transmission maxima or minima in the spectrum and using that $d = 1/(2 n \Delta k)$.

In **Paper IV** optical transmission spectra of spin coated metal-nanoparticle inks on glass were also measured using the absorption spectrophotometer. Measurements of the absorbance, reflectance and transmittance of paper samples with and without ink-jet printed silver were, however, made by using an experimental setup consisting of an integrating sphere, a xenon lamp and a fibre optics spectrometer (USB2000, Ocean Optics Inc.) connected to a computer.

4.3.3. Other techniques

Among the other characterization techniques that were used are X-ray photoelectron spectroscopy (XPS), AFM, scanning electron microscopy (SEM) and Kelvin probe measurements. XPS (Quantum 2000 scanning spectrometer, Physical Electronics) was used in order to investigate the semiconductor coverage on the printed source and drain contacts in **Paper II**. A monochromatic Al K α X-ray source was used, and the atomic concentration of the different elements was determined by calculating the area of the peaks and correcting for the sensitivity factors. The Kelvin probe technique was used for measuring the work function in room atmosphere of evaporated silver as a function of air exposure and also of ink-jet printed silver structures. AFM (AutoProbe CP, Park Scientific Instruments, and Caliber Scanning Probe Microscope, Veeco Instruments Inc.) was used for investigating the surface of the substrates, the ink-jet printed silver electrodes and the P3HT and PVP layers. The viscosity of the inks was measured using a Bohlin VOR Rheometer.

5. Results and discussion

5.1. Printed HIFETs on plastics

5.1.1. Reverse gravure coated HIFETs

In **Paper I** we demonstrated the possibility of using the roll-to-roll reverse mode gravure coating technique for subsequently applying the homogeneous semiconductor and insulator layers of a low-voltage OFET on a low-cost plastic substrate. This is the first time to our knowledge that the reverse gravure coating method has been used for fabricating transistors. In Paper 12 we have also shown for the first time that this technique also can be used for fabricating organic solar cells with a similar performance to that of spin coated ones.

The dry coating thickness could be controlled mainly by changing the gravure roll, the web and roll coating speeds and the ink concentration. An engraved roll consisting of 47 grooves/cm was rather suitable for coating both the semiconductor and the gate dielectric. The solutions that finally were used consisted of 9 mg/ml of P3HT in toluene and 100 mg/ml of PVP in ethylacetate, and the viscosity was measured to around 1 mPas and 5 mPas, respectively. Initially, there was a problem with the semiconductor layer partially being removed from the Melinex 505 film when the insulator was gravure coated on top. This was, however, solved by changing the substrate to a thinner and rougher polyester film (Mylar A).

The thickness of the P3HT and PVP coatings was obtained from the measured absorption spectra (see Section 4.3.2), and is shown in Figure 5.1 as a function of the web speed. The coating thickness was found to increase with the web speed at a constant roll speed, except for at higher web speed to roll speed ratios, where the thickness seemed to saturate and even decrease when using the higher viscosity PVP-ink. In contrast to these results, Hewson et al. when studying the reverse gravure coating technique did not see any increase in the coating thickness with an increasing web-to-roll speed ratio, but only a constant or slightly decreasing coating thickness [148,149]. This difference is probably due to the low viscosity of the ink and the low coating speed that was used in our work causing some of the ink in the grooves to be poured back into the container by the gravitation before reaching the web. Consequently, the maximum coating thickness that can be achieved by increasing the web speed is larger for larger roll

5. Results and discussion

speeds when using a low-viscosity ink and a relatively large groove size. Furthermore, the pickout fraction (see Section 4.2.2) of the low-viscosity P3HT-ink (of up to 35 %) was found to be lower than that of the more viscous PVP-ink (up to 70 %) when using the same coating speeds, which also could be explained by the grooves of the gravure roll not being completely filled when using the low-viscosity ink at low roll speeds. The low ink viscosity and surface tension also explains why the otherwise expected coating instability “streaking”, that is caused by starvation at web-to-roll speed ratios of above 1.1–1.2 [148,149], was not observed in this work.

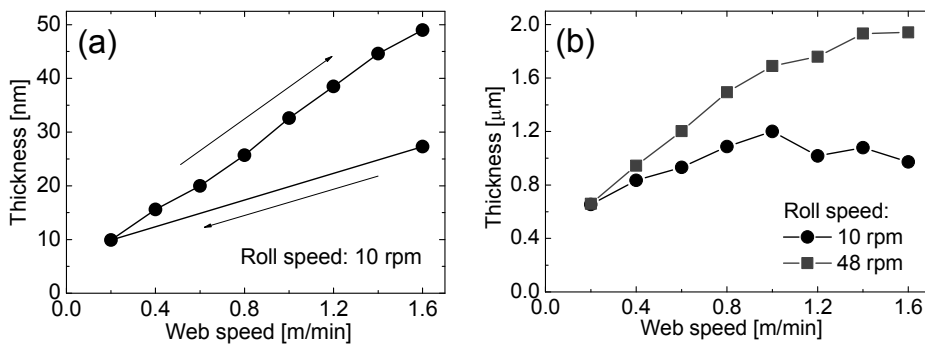


Figure 5.1. The measured dry thickness of the reverse gravure coated layers of (a) P3HT and (b) PVP are shown as a function of the web speed. The arrows in (a) indicate the order in which the P3HT-coatings were applied. The roll speed of 10 rpm corresponds to a roll surface speed of around 0.6 m/min. [Paper I]

When comparing the first and the last P3HT-coating in Figure 5.1 (a) a large difference is seen for the same coating parameters. This discrepancy could be explained by the evaporation of solvent during the coating experiment of several meters resulting in a higher ink concentration and an increased viscosity. The same effect was not seen when coating the PVP-ink, and the faster evaporation of the P3HT ink could be ascribed to the use of the specially made low-volume containing (≈ 10 ml) ink tray. A more constant ink concentration could be ensured by using a lower evaporation rate solvent, by continuously filling the ink container or by replacing the open ink tray with a chambered doctor blade.

The P3HT and PVP layers used in the transistor structures were reverse gravure coated at a web speed of 1.6 m/min and a roll speed of 10 and 20 rpm, and the thickness was measured to 30 nm and 1.6 μm , respectively. In Figure 5.2

5. Results and discussion

the transistor characteristics of a HIFET made by spin coating the P3HT and PVP layers are compared to those of reverse gravure coated ones with the gate contact being applied by drop casting or ink-jet printing.

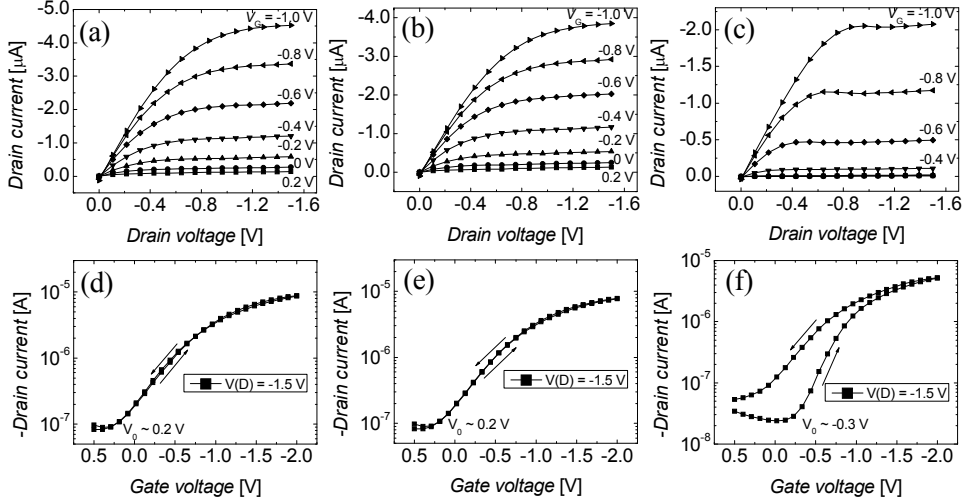


Figure 5.2. The measured (a–c) output and (d–f) transfer characteristics of HIFETs fabricated by (a,d) spin coating or (b,c,e,f) reverse gravure coating the polymeric semiconductor and the gate dielectric are shown. The gate electrodes were applied by (a,b,d,e) drop casting or by (c,f) ink-jet printing. The channel width and length of the HIFETs were 1.5 mm and 35 μm , respectively. [Paper I]

The reverse gravure coated HIFET in Figure 5.2 (b,e) have a very similar characteristics to that of the spin coated one (a,d). A larger difference is, however, seen in the characteristics of the HIFET with an ink-jet printed gate electrode (c,f). The hysteresis is clearly visible, and both the turn-on voltage and the on-current are lower. The same PEDOT:PSS-ink was used, but it was diluted with water (1:1) and a surfactant was added in order to make it inkjettable. The inkjetting procedure resulted in a thinner PEDOT-layer than by drop casting and possibly also in partial intermixing with the PVP-layer. The larger resistance and electrochemical doping and dedoping of the gate electrode could explain the larger hysteresis of the HIFET with the inkjetted gate.

5.1.2. Fully printed HIFETs

In **Paper II** we showed that HIFETs can be completely fabricated by using roll-to-roll compatible printing and coating techniques. The reverse gravure coating technique introduced in **Paper I** was used for applying both the semiconducting and the insulating layer, while all the contacts were applied by ink-jet printing. In Figure 5.3 a schematic image of the structure of an all-printed HIFET and of the manufacturing process is shown together with an optical microscope image of the final devices. To our knowledge, this is the first demonstration of a fully printed low-voltage OFET.

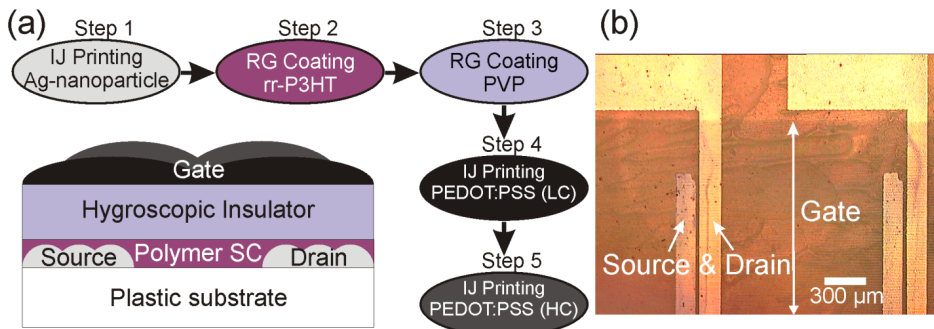


Figure 5.3. The five-step manufacturing process and the structure of the HIFET is schematically shown in (a), while a top-view optical microscope image of two fully printed transistors is shown in (b). Following abbreviations are used: semiconductor (SC), ink-jet (IJ), reverse gravure (RG) and low- and high-conducting (LC and HC). [**Paper II**]

The source and drain electrodes consisted of an ink-jet printed commercial silver nanoparticle ink that turned highly conducting after thermal annealing at 120 °C for 20 min. The distance between the source and drain electrodes (L) was around 40 μm and the overlapping width (W) was 1.5 mm. The otherwise relatively common coffee-stain effect in ink-jet printing was not seen on the source and drain contacts. The thickness of the P3HT and PVP layers was determined from the absorption spectra to around 30 nm and 1.2–1.3 μm, respectively. The gate electrode was applied by inkjetting two different commercially available PEDOT:PSS inks (see Section 4.1.2). Since the highly conducting PEDOT-ink contained ethanol that would dissolve the non-crosslinked PVP-layer, a thin layer of the less conducting inkjettable aqueous PEDOT-ink was first applied as a barrier layer.

5. Results and discussion

The output and transfer characteristics of an all-printed HIFET are shown in Figure 5.4. The somewhat degraded characteristics after 48 days in ambient air can be partly explained by the increased resistance of the PEDOT-gate, but partly also by the reduced ion conductivity of the dried PVP layer.

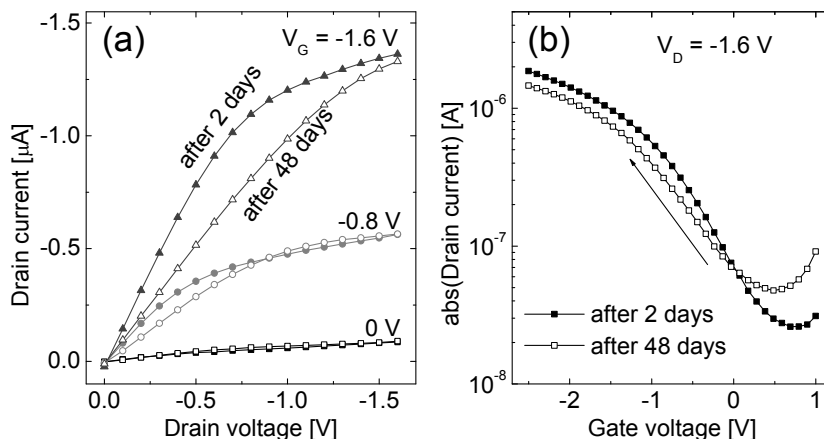


Figure 5.4. The output (a) and transfer (b) characteristics that were measured 2 days and 48 days after the fabrication of an all-printed HIFET are shown. [Paper II]

The current levels of the fully printed HIFETs were slightly lower than that of HIFETs with evaporated gold source and drain contacts of similar channel dimensions in Paper I. Although the inkjetted silver source and drain contacts were relatively thick (200–400 nm) in comparison to those with evaporated gold ($\approx 30\text{ nm}$), this did not have a clear effect on the gate leakage currents that remained below 1/100 of the drain currents. Furthermore, since the inkjetted source and drain contacts were substantially thicker than the semiconductor layer, poor coverage of the semiconductor resulting in a large contact resistance could be expected [159]. However, no effect from the contact resistance was seen in the transistor characteristics, and XPS measurements verified a complete P3HT-coverage by showing no signal from the underlying silver contacts. The homogeneous semiconductor coverage was explained by the low surface energy of the P3HT-solution and by the properties of the reverse gravure coating technique.

5. Results and discussion

A lower transistor performance could also be expected by the change in the material of the source and drain material from gold (in **Paper I**) to silver causing an increased hole injection barrier. While the work function of gold (around 5.2 eV) is very close to the ionization potential of P3HT of around 5 eV, the work function of silver is significantly lower (around 4.3 eV [160]). However, the Kelvin-probe measurements in air showed that the work function of the silver contacts actually was around 0.3 eV higher than that of a gold surface. This difference was explained by the hydrocarbon adsorption on gold in air that has been reported to reduce the work function to around 4.5 eV [161,162], and by the formation of silver oxide on the silver contacts resulting in an increase in the work function of silver (by 0.4–0.7 eV) [163,164]. The presence of oxygen on the sintered ink-jet printed silver contacts was confirmed by XPS, showing similar amounts of silver, oxygen and carbon on the surface, while no oxygen and only 15 % of carbon was detected in the bulk after sputtering with argon ions. Consequently, by taking this effect into account, the value of the work function of the sintered silver nanoparticles in air is not far from the ionization potential of P3HT.

In addition to the relatively low hole injection barrier, the low contact resistance can also be explained by the staggered (top-gate bottom-contact) FET-geometry that was used, which allows charge injection from the source and drain contacts into the semiconductor over a larger area. Furthermore, a reduced contact resistance by two orders of magnitude has recently been demonstrated in ion-modulated OFETs upon electrochemical doping of the semiconductor [48].

5.1.3. Insensitivity to substrate roughness of the HIFET

The use of a polyester substrate with a relatively large surface roughness (25–50 nm) was motivated by the better adhesion of the P3HT-layer to this substrate than to a smoother one (4–6 nm). However, while fully printed HIFETs operate properly also on a relatively rough plastic substrate, as is shown in Figure 5.5, this is not the case with conventional OFETs, where an increase in the surface roughness of the semiconductor-dielectric interface typically leads to a strongly reduced transistor performance [86,165–168].

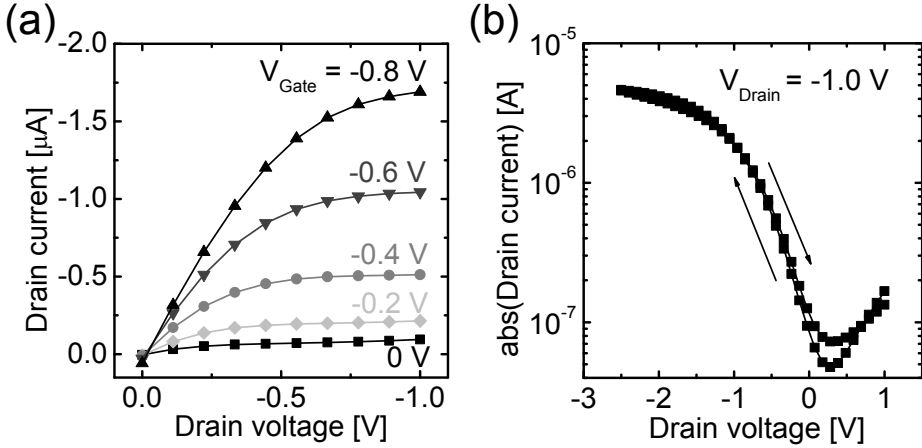


Figure 5.5. The (a) output and (b) transfer characteristics of a fully printed HIFET on a relatively rough low-cost plastic substrate are shown [Paper III]. The transistor operates at only 1 V and was fabricated in the same way as in Paper II.

In Figure 5.6 the transfer characteristics of HIFETs and conventional OFETs fabricated on two polyester substrates with different roughness are compared. The transistors were fabricated with the same channel geometry by thermal evaporation and spin coating, but the thickness of the PMMA and PVP layers was around $0.8 \mu\text{m}$ and $1.5 \mu\text{m}$ in the conventional OFET and HIFET, respectively. While the characteristics of the HIFETs were very similar on both substrates, the conventional OFET exhibited a lower on/off ratio and a lower slope of $\sqrt{I_D}(V_G)$ on the more uneven polyester film. Considering that this slope is proportional to the square root of the capacitance and the charge carrier mobility in the saturation region (see Equation 2.3), the lower value of the conventional OFETs on the rougher plastic substrate can be ascribed to a reduced mobility if assuming that the capacitance across the gate dielectric is similar on both substrates. A second effect of a larger surface roughness is the increasing risk for electric breakdown of the gate dielectric, which partly explains why the yield of working devices of the conventional OFETs was lower on the rougher substrate than on the smoother substrate. Because of the thicker PVP layer and the low-voltage operation, this was not the case for the HIFETs, showing a yield of above 70 % on both substrates and a lower statistical variation.

5. Results and discussion

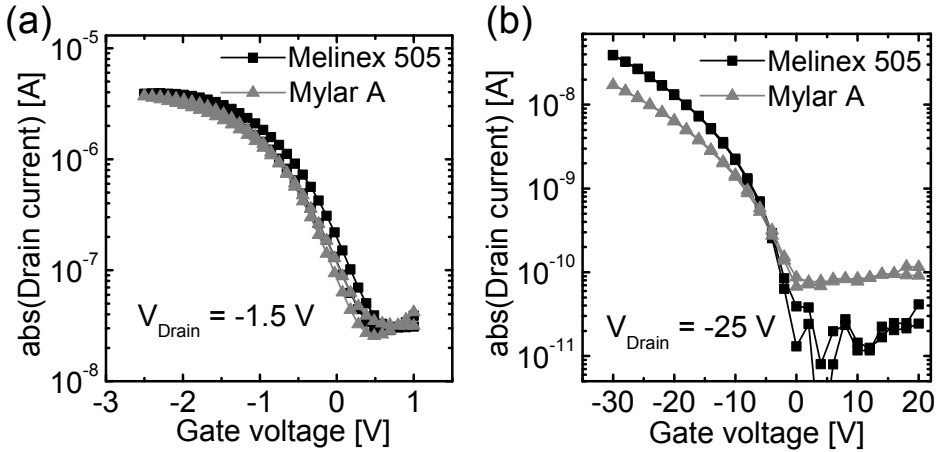


Figure 5.6. The transfer characteristics of (a) a HIFET and (b) a conventional OFET that have been fabricated on the smooth Melinex 505 and the more uneven Mylar A substrates are shown for comparison. [Paper III]

The insensitivity of the HIFET to the surface roughness can be understood by comparing the electric field distribution inside a gate dielectric based on a polyanionic electrolyte with that in a conventional electrical insulator (see Figure 2.2). In a conventional OFET, the electric field from the gate is higher on the parts of the semiconductor channel that are closer to the gate contact and lower on the areas in the “valleys”, which results in low charge-carrier mobility. In an ion-modulated OFET (e.g. the HIFET), on the other hand, the ions will form a thin electric double layer also at the “valleys” of the semiconductor interface, which results in an almost equally large electric field over the whole semiconductor channel area, and consequently little effect on the charge carrier mobility. An additional reason for the insensitivity to the surface roughness is the relatively high capacitance across the hygroscopic insulator layer, which results in a high charge carrier density in the semiconductor and filling of the trap states.

The results in **Paper III** demonstrate the robustness of the HIFET enabling the use of low-cost plastic substrates with a relatively rough surface. This discovery was also an inspiration to turn to an even rougher type of substrate; paper.

5.2. Printed electronics on paper

5.2.1. IR-sintering of printed metal-nanoparticles on paper

Printable conductors with a high conductivity are desired in most flexible electronic applications, e.g. as wires and contacts for transistors. Similar structures with a relatively small feature size can be achieved by first ink-jet printing a metal-nanoparticle ink and then applying a thermal sintering process. However, while the metal-nanoparticle inks can be printed in a roll-to-roll process, most of the sintering techniques that can be used on low-cost flexible substrates require long annealing time and are incompatible with a fast roll-to-roll manufacturing process. A roll-to-roll compatible sintering process of ink-jet printed silver- and gold-nanoparticles on paper by using low-cost incandescent lamps was, nevertheless, demonstrated in **Paper IV**. While low-cost plastic substrates are quickly deformed by the light absorbed from the lamps, the method is especially suitable on paper substrates thanks to the relatively high thermal stability, low thermal conductivity and high diffuse reflectance of paper. A new way of deriving the light absorptance, transmittance and reflectance of a substrate from intensity measurements by using an experimental setup with an integrating sphere was developed, and the absorptance was found to be around ten times larger on inkjetted silver structures than on a clean paper surface.

In Figure 5.7 the measured volume resistivity of inkjetted silver nanoparticles on paper is shown as a function of the exposure time to an incandescent lamp. A volume resistivity of down to 10–20 $\mu\Omega\text{cm}$ was reached within 5–15 s of IR-exposure (at an intensity of 2–4 W/cm^2), which corresponds to around ten times the bulk resistivity of silver (1.6 $\mu\Omega\text{cm}$). This is a very low resistivity level, especially considering the use of a paper substrate and the relatively small thickness (<500 nm) of the printed silver structures. While the volume resistivity continued to decrease after more IR-exposure, too long irradiation should not be applied, since the paper surface was degraded and turned yellow-brown after more than 15 s. Using the same IR-sintering setup for sintering inkjetted silver nanoparticles on a glass substrate, a longer exposure time than on paper, of up to 1 min, was required in order to achieve conducting structures. This can be explained by the larger thermal conductivity and thickness of glass than of paper and by the lower light absorptance of the printed silver structure on glass than on paper. The silver film on paper was more

5. Results and discussion

uneven than on glass or plastics, which also explains the larger reflectance of the silver film on plastics than on paper.

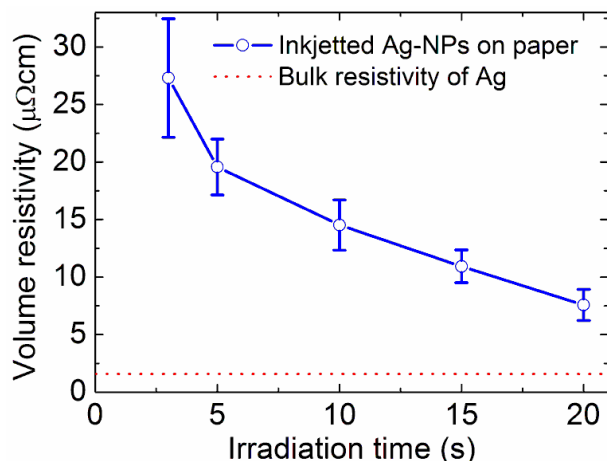


Figure 5.7. The measured volume resistivity of ink-jet printed silver structures on paper is shown as a function of the exposure time to the IR-lamp. The bulk resistivity level of pure silver is indicated with the dashed line. [Paper IV]

A relatively high print resolution was achieved both on plastics and paper when printing the silver nanoparticle ink. Optical microscope images of ink-jet printed interdigitated silver contacts on both plastics and paper are shown in Figure 5.8.

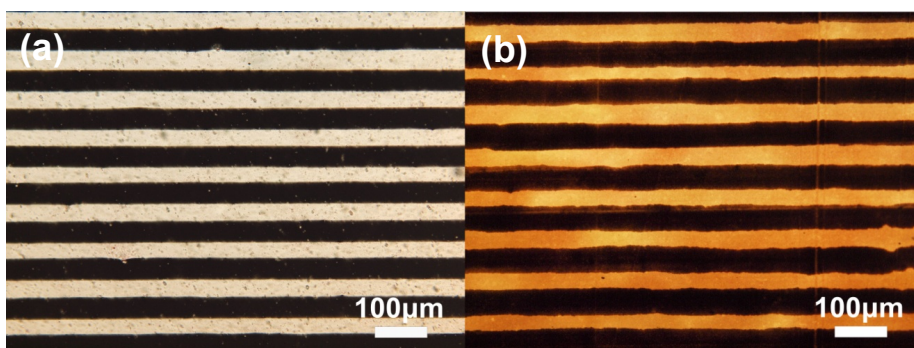


Figure 5.8. Optical microscope images of ink-jet printed interdigitated silver contacts are shown (a) on a polyester film and (b) on a paper substrate. The contrast in the images was enhanced by illuminating from below the substrates, which explains the dark colour of the printed structures. [Paper IV]

5. Results and discussion

The distance between the contacts was around 33 μm on both substrates, while the line-edge roughness was around 1.6 μm and 4.6 μm on plastics and paper, respectively. The larger lateral variation on paper than on plastics can be explained by the larger topological and surface energy variations on paper. When using these interdigitated structures as source and drain contacts for OFETs, the larger channel length variation on paper could possibly affect the final transistor characteristics adversely by reducing the on/off ratio and the saturation in the output characteristics. A higher print resolution could be achieved by further optimizing the print parameters or substrate, but there is typically a trade-off between the manufacturing speed and the achievable print resolution.

Silver is typically preferred over gold because of the material cost, but there may still be applications where printed gold nanoparticles are more suitable. However, the coffee-stain effect, as well as crack formation during sintering, was seen when inkjetting a gold nanoparticle ink. Both effects were, nevertheless, found to be strongly reduced on paper as compared to glass or plastic substrates, which was partly explained by the porosity of paper that allows penetration into the substrate of solvents and decomposed alkanethiols. By ink-jet printing dodecanethiol protected gold nanoparticles and applying subsequent IR-sintering on paper, a volume resistivity of down to 25 $\mu\Omega\text{cm}$ was obtained, which corresponds to around ten times the bulk resistivity of pure gold.

5.2.2. HIFET on a recyclable paper substrate

In order to fabricate working HIFETs on paper it is not enough to be able to print the highly conducting contacts with a relatively high print resolution as was shown in **Paper IV**, but it is also important that a thin continuous semiconductor layer can be applied without too much absorption into the substrate and that the surface roughness is low enough to enable the formation of a homogeneous electronic insulating layer. While this could be achieved by coating or laminating with a plastic film, this would compromise the low-cost and recyclability of the paper substrate. In order to maintain the recyclability and low-cost of paper, our approach in **Paper V** of tuning the surface properties for printed electronics is to use conventional ways of coating aqueous dispersions of pigments and binders and by calendaring.

5. Results and discussion

In Figure 5.9 a cross-sectional SEM image of a recyclable multilayer coated paper substrate that was used as a substrate for the HIFET is shown. The paper was coated in laboratory scale by blade, rod and reverse gravure coating, but paper substrates with a similar layer structure were later also fabricated in industrial trials by curtain coating [Paper 1]. RMS surface roughness down to 55 nm was measured after calendering the multilayer pigment coated paper substrates (see Section 4.1.1), which was comparable to the surface roughness of a low-cost plastic substrate.

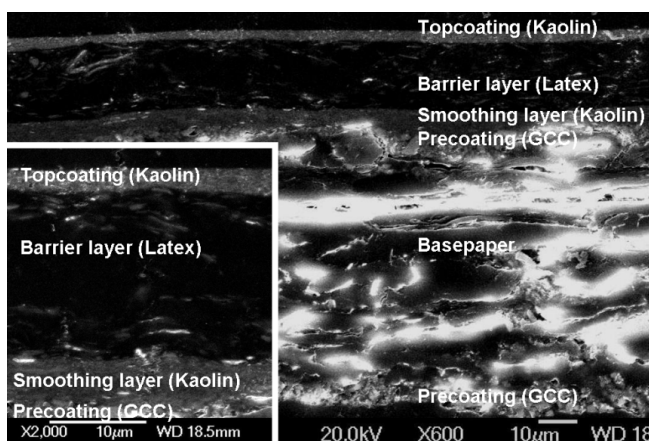


Figure 5.9. A cross-sectional SEM image of the structure of a multilayer coated paper substrate is shown together with a higher magnification image in the inset. [Paper V]

The barrier properties were also studied. A slowly evaporating dilute solution of P3HT in dichlorobenzene was found to fully penetrate all of the tested paper substrates except for those including a latex-barrier layer. However, excessive ink spreading and the undesirable coffee-stain effect were seen on the paper substrate with the latex based barrier layer on top, as well as on a plastic substrate. Nevertheless, when an additional thin mineral pigment based top layer was coated onto the latex barrier (see the structure in Figure 5.9), both the excessive spreading and the coffee stain effect were prevented, while the good barrier properties remained. The thickness and porosity of the top mineral layer controls the absorption of ink solvents, and could be optimized for different applications. The water vapour transmission rate of the used paper substrate was measured to around 10 g/m²/day (at 23 °C and 85 % relative humidity).

5. Results and discussion

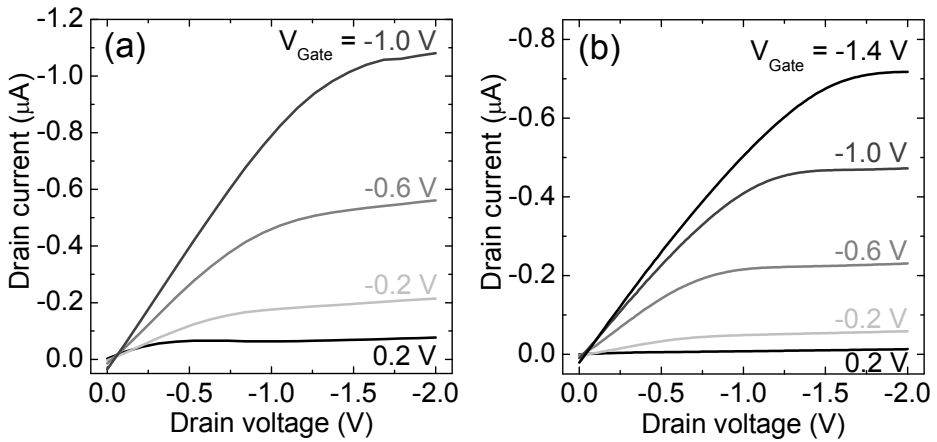


Figure 5.10. The output characteristics of a HIFET on paper that were measured (a) directly after the fabrication [Paper V] and (b) after 5.5 months of storing in ambient air [Paper 10] are shown. The channel width was 1.5 mm and the channel length around 40 μm .

HIFETs were fabricated on the paper substrate by IR-sintering the ink-jet printed silver-nanoparticle source and drain electrodes, spin coating the P3HT and PVP solutions and drop casting the gate contact. The output characteristics of the first reported low-voltage enhancement mode organic transistor to be fabricated on a paper substrate are shown in Figure 5.10. The HIFET still worked after 5.5 months, but the current levels in the output characteristics had decreased by a factor of around two.

HIFETs with a better performance was later fabricated by replacing the semiconductor P3HT with PQT-12 that has a higher ionization potential, which resulted in lower off-currents because of inhibited oxygen doping [Paper 5, Paper 6]. However, the charge carrier mobility was typically lower when using PQT-12 instead of P3HT. This was compensated by ink-jet printing interdigitated source and drain structures with a larger channel width over length ratio, which also resulted in an improved drain to gate current ratio. In Figure 5.11 the typical output and transfer characteristics of HIFETs fabricated using this approach on paper and on plastics are compared.

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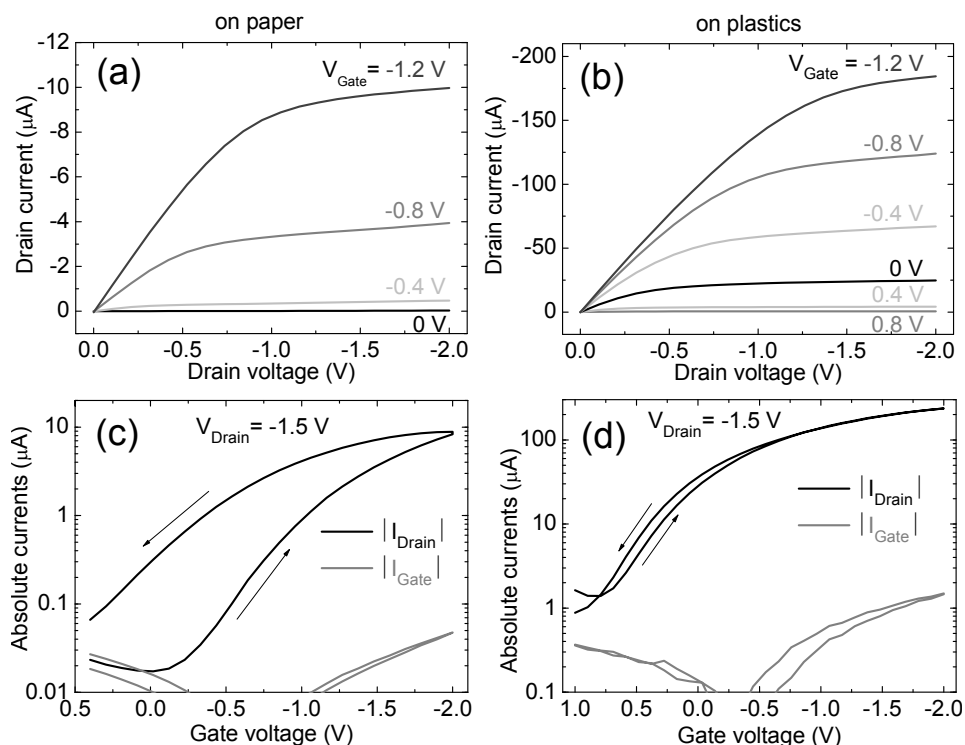


Figure 5.11. The (a,b) output and (c,d) transfer characteristics of a HIFET (a,c) on paper is compared to that (b,d) on a plastic substrate. The PQT-12-layer was applied by ink-jet printing on paper, while it was spin coated on the polyester substrate. The channel length was around 40–50 μm and the channel width was $10 \times 2.5\text{ mm}$ on paper and $20 \times 2.5\text{ mm}$ on plastics. [Paper 6]

HIFETs on both paper and plastics operate at low-voltages and show an on/off-ratio of 10^2 – 10^3 . The turn-on voltage of transistors on paper was closer to 0 V than on plastics, but the hysteresis in the transfer characteristics was much larger and the transistor currents around ten times lower. Among the factors that could explain these differences in the transistor performance are the semiconductor coverage and ordering, roughness of the semiconductor-dielectric interface and electrochemical effects on/from the paper substrate. The poor semiconductor coverage on the paper substrate was confirmed by XPS measurements showing a strong signal of aluminium, silicon and oxygen from the underlying paper surface. The penetration of the low concentration slowly evaporating organic semiconductor solution into the surface layer of the pigment coated barrier

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paper also explains why more than twice as much ink-jet printed semiconductor material was required on paper than on plastics in order to achieve working transistors. The same amount of semiconductor material would correspond to a dry homogeneous film with a thickness of around 80 nm and 30 nm for paper and plastics, respectively. The penetration into the paper substrate could be further reduced by using inks that have a higher concentration and evaporation rate.

The multilayer coated paper can also be used for various sensors [Paper 3, Paper 10], and the printability for other functional inks can be tuned by adjusting thickness and porosity of the top coating. While HIFETs fabricated on paper with a thin kaolin-based top layer typically showed the best performance, better flexography printing of particle-based inks was achieved on thicker and more porous papers with precipitated calcium carbonate or porous silica in the top layer [Paper 1, Paper 4]. Working HIFETs have also been fabricated on a commercial paper (Magnostar, SAPPI) [Paper 2]. However, on this substrate, the semiconductor actually penetrated all the way to the back side.

5.3. Challenges and outlook

Similar on-current levels of the fabricated HIFETs should be expected after taking into account the different channel dimensions by normalizing the current with the channel width to length ratio (of 15–1000), but instead a very large variation is found with values ranging from 0.2 to 200 nA (at voltages of around -1.5 V). Among the main factors affecting the normalized on-currents of the studied transistors are the semiconductor material and thickness and the substrate used. It turns out that the normalized on-currents of the fabricated transistors are around ten times lower when using paper instead of plastics, as well as when using PQT-12 instead of P3HT.

While a lower performance of transistors made on paper instead of plastics may be acceptable for some applications, there are also ways of improving the HIFETs on paper. A rather interesting approach of improving the charge carrier mobility of OFETs on paper is to utilize the phase separation of polymer semiconductor-insulator blends [169–172]. Vertical phase separation of P3HT to the surface can be obtained when mixing with a polymer insulator, such as PMMA, because of the lower surface energy (and solubility) of P3HT than that of PMMA ($21 \text{ mJ/m}^2 < 46 \text{ mJ/m}^2$). Similar on-currents as on plastics were obtained by using this approach on paper with a P3HT to PMMA ratio of 1 to 4–9, which could be explained by the better semiconductor coverage and ordering and by the barrier layer towards ionic species in the paper. Fortunately, the vertical phase separation was not fully homogeneous on the silver contacts, since Ohmic contact was obtained between the bottom source and drain contacts through the semiconductor layer.

In addition to improving the transistor performance, one of the remaining goals is to fabricate electronic circuits in a continuous roll-to-roll process. We are currently using a custom-built hybrid printing machine consisting of different printing units (see Section 4.2.3), which enables HIFETs to be fully manufactured in a roll-to-roll process. In the Funprinter the source and drain contacts are typically applied by flexo printing a flake based silver ink that does not require as high annealing temperature as nanoparticle inks. The print resolution of the flexo printed source and drain contacts (see Figure 5.12 a) was, however, much lower than what was achieved by ink-jet printing. The flexo printed structures were also thicker, more uneven and had a much larger surface roughness with even micrometer-high peaks. It was, nevertheless, still possible to fabricate working HIFETs even with flexo printed contacts having a channel

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length of up to 300 μm [Paper 1, Paper 4]. The output characteristics of such a transistor are shown in Figure 5.12 (b). Spray coating was used in the roll-to-roll process for applying the semiconductor in order to reduce the absorption into the paper substrate. The large size of the transistors is unsuitable for most practical applications, but was used because of the limited print resolution and in order to simplify the registration when printing the gate contacts.

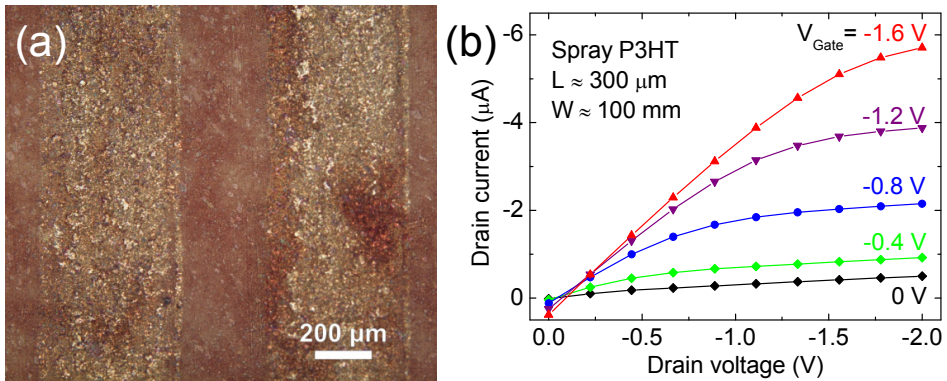


Figure 5.12. An optical microscope image of flexography printed source and drain structures is shown in (a). The red/purple colour originates from the spray coated P3HT. The output characteristics of a HIFET with large channel dimensions are shown in (b).

An important challenge when fabricating the HIFETs in a roll-to-roll process is how to apply the gate contact without having problems with large gate leakage currents. Flexo printing with a very low print pressure or roll-to-roll ink-jet printing of aqueous PEDOT-inks have been found to work rather well on a reverse gravure coated PVP layer [Paper 1]. However, if the PVP-layer is too thin, there are typically problems with gate leakage, because of the large surface roughness of the flexo printed source and drain contacts and the partial dissolution of the PVP-layer by the printed PEDOT-ink. If the PVP-layer, on the other hand, is too thick, there are often problems with crack formation during the drying process causing electrical shortage when the gate contact is applied. This effect could be prevented by dispersing kaolin particles into the PVP-solution [Paper 1, Paper 4]. When printing electronic circuits, simple interconnections and patterning of the PVP-layer may also be required.

Among the low-cost low-voltage low-speed applications where this kind of printed transistor circuits could be used are for logics and amplification of

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signals from printed sensors. Efforts should, however, be put into reducing the statistical variation in the performance of the printed HIFETs. For practical applications, another important concern is the stability of the transistors. The long-term degradation of HIFETs was briefly discussed in **Paper II**. A related and relatively common issue is the gate-bias stress during the operation of FETs, which results in a decreasing drain current in the on-state or, correspondingly, a negative shift in the threshold voltage. In case of the HIFET, especially large effect is seen at a high relative humidity and when applying a high voltage to the gate. However, if the HIFET is operated at a relative humidity of around 30 % and the gate voltage is kept at around 1 V, the effect is comparable to that of conventional OFETs.

6. Summary

The main advantage of organic electronics over the inorganic counterparts lies not in any electrical performance, but rather in the solution processability that opens up for low-cost flexible electronics fabricated by using printing techniques. Replacing the commonly used laboratory scale fabrication techniques with mass-printing techniques is, however, truly challenging, especially when low-voltage operation is required. It was, nevertheless, shown in **Paper II** that low-voltage organic transistors can be fully printed with a similar performance to that of transistors made by laboratory scale techniques. The use of an ion-modulated type of OFET, not only enabled low-voltage operation and printability, but was also found to result in low sensitivity to the surface roughness of the substrate in **Paper III**. This enables not only the use of low-cost plastic substrates, but even the use of paper as a substrate.

While the porosity of and absorption into the paper substrate is advantageous in a graphical printing process, by reducing the spreading and the coffee-stain effect and by improving the adhesion, this also provides great challenges when applying thin electrically active layers. In **Paper V** we were, nevertheless, able to demonstrate the first low-voltage OFET to be fabricated on paper. We also showed in **Paper IV** that low-cost incandescent lamps can be used for sintering printed metal-nanoparticles, and that the process was especially suitable on paper and compatible with a roll-to-roll manufacturing process.

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Svensk resumé

I princip all elektronik idag bygger på kiselbaserade transistorer. Det finns dock intressanta potentiella tillämpningar där de konventionella transistorerna inte är optimala. Så är fallet för billiga och böjbara elektroniska applikationer som t.ex. displayer, sensorer och smarta etiketter.

Plaster, som är både billiga och flexibla, har oerhört stora användningsområden. I elektronik används dessa polymerbaserade material främst som isolering. Upptäckten att vissa konjugerade polymerer också kan leda ström, vilken belönades med Nobelpriset år 2000, har dock gjort det möjligt att också tillverka polymerbaserade transistorer. Till skillnad från konventionella oorganiska transistorer kan dessa billiga och flexibla organiska transistorer tillverkas utgående från lösningar och vid låga temperaturer, vilket i princip möjliggör en snabb och billig masstillverkningsprocess på stora flexibla plast- och papperssubstrat genom att använda olika trycktekniker. Jämfört med grafisk tryckning ställer dock tryckning av plastelektronik helt nya krav på tryckprocessen. I avhandlingen visar jag att det trots allt är möjligt att enbart med hjälp av trycktekniker tillverka polymerbaserade transistorer med liknande prestanda som uppnås vid tillverkning med laboratorietekniker.

Eftersom de flesta tillämpningarna är tänkta att drivas av batterier eller solceller, alternativt genom elektromagnetisk induktion, bör transistorerna dessutom fungera vid låga spänningar, vilket är en stor utmaning för organiska transistorer. Den typ av transistor som jag har arbetat med är jonmodulerad, och kan drivas vid låga spänningar tack vare att isolatorlagret mellan gate-kontakten och halvledaren består av en hygroskopisk polymer som fungerar som en elektrolyt i normal luftfuktighet, vilket resulterar i en hög kapacitans genom de elektriska dubbellager som bildas vid gränsskikten.

I avhandlingen visar jag också att dessa jonmodulerade organiska transistorer inte bara är lämpliga för tryckning, utan dessutom förhållandevis okänsliga för ojämnheter på plastsustraten, och t.o.m. kan tillverkas direkt på papperssubstrat.